Course Focus

- Focus:
  - Circuit design for modern electrical interfaces

- Interfaces (links) are now complex, mixed-signal communication systems
  - Will do a lot of transistor-level design
  - But will be tightly coupled to system-level design

- Goal:
  - Learn how to design an optimized link given a target application
Administrative

- Course web page:
  http://bwrc.eecs.berkeley.edu/classes/icdesign/ee290c_s11

- Webcast link:
  http://webcast.berkeley.edu

- Office hours
  - 519 Cory Hall
  - Tues. 9-10am, Thurs. 11am-12pm

- All announcements made through web page
  - Check back often

Course Prerequisites

- Minimum: EE141, EE240
  - EE241 helps too, but not necessarily required

- Assume you are familiar with:
  - Basic data converters (at level of EE240 project - EE247 not required)
  - Verilog/VHDL
  - Basic transmission lines (EE117)

- Exposure to communications & signal processing helpful
  - But deep expertise not required – will cover important points of what we need
Lecture Notes

• Based on slide from Prof. Borivoje Nikolic, Prof. Vladimir Stojanovic (MIT), Jared Zerbe (Rambus), and myself

• Primary source of material for the class
  • No required text

• Notes posted on the web at least 1 hour before lecture
  • Will hand out limited # of hard copies in class

Some References

• Digital Systems Engineering

• Design of High-Performance Microprocessor Circuits
  Edited by A. Chandrakasan, W. J. Bowhill, F. Fox, IEEE Press, 2001
  • Chapter on high-speed signaling and I/O design

• Design of Integrated Circuits for Optical Communications
  B. Razavi, McGraw-Hill, 2002

• Papers from:
  • IEEE Journal of Solid-State Circuits
  • IEEE International Solid-State Circuits Conference
  • IEEE Symposium on VLSI Circuits
  • IEEE Custom Integrated Circuits Conference
  • …
Grading

- Grading:
  - HW: 30%
    - Will have 3-4 assignments
    - Essential for learning the class material
  - Project: 60%
    - Will design a complete high-speed (>10Gb/s) interface
    - Groups of 3-4
      - Will want wide range of skills - form your groups now
  - Presentations: 10%
    - Will give two project-related presentations
    - First at project “half-way” point
    - Second at project end

- No exams
  - But don’t take course lightly – will be a lot of work

Homework

- Homework:
  - Can discuss/work together
  - But write-up must be individual
  - Drop in box outside Elad’s office (519 Cory)
  - Generally due 5pm on Thursdays

- No late submissions
  - Start early!
Schedule Notes

• ISSCC Week: 2/21 - 2/25 (no lectures)
• Spring break: 3/21 – 3/25
• Project:
  • Will be broken into 3-4 parts
  • Check on the website for updates
  • First presentations: ~1st week of April
  • Final presentations: RRR week

Shouldn’t This Be Really Easy?

• This really is a “link“
  • (Although maybe not the best one)
• Seems like it should be really easy to build
  • So why have this class at all?
• Look at where/how links are really used
Lots of Data on the Move

Links Are Everywhere
Inside of a Router (ca. 2006)

- Line Cards: 8 to 16 per System
- Passive Backplane
- Switch Cards: 2 to 4 per System

- OC-192
- 10Gb/s Laser driver link
- 4x3.125 Gb/s XAUI Serial Links (chip-to-chip)
- 3.125-12.5Gb/s Backplane Serial Links

Inside of a Router (ca. 2011)

- Line Cards: 8 to 16 per System
- Passive Backplane
- Switch Cards: 2 to 4 per System

- OC-768
- 40Gb/s Laser driver link
- 4x10 Gb/s Serial Links (chip-to-chip)
- 6.25-25Gb/s Backplane Serial Links

- No extra wires/cables, minimal changes to PCB
- But everything needs to run faster…
Not Just Routers…

- Chip-to-chip signaling
  - Computers, games:
    - DDR, DDR2: 100-400Mb/s
    - RDRAM 800-1600Mb/s
    - XDR DRAM 3.2-6.4Gb/s

- Board-to-board signaling:
  - Computers, peripherals:
    - PCI (66-133-400MHz), PCI Express (2.5Gb/s – 10Gb/s)
    - USB (10Mb/s – 10Gb/s)

- Constant desire to signal faster at same or lower power
  - No matter where the links are

So What Was Wrong With This?

- In principle, nothing 😊
  - As long as the wire is “short enough”
  - And get the “right” clock at both TX and RX

- When is a wire “short enough”?  
  - How to get the “right” clocks?
What a Link Needs to Do

- Get bits from the TX to the RX (Signaling)

- Determining which bit is which (Timing)

Backplane Signaling At 2-3Gb/s (Past)

- Other than knowing about transmission lines
  - “Wire” (channel) wasn’t an issue up to 2-3Gb/s
  - “Good old days” – on-chip circuits set speed limits
  - Lots of publications on how to make them faster
Backplane Signaling At 10+Gb/s (Today)

- Channel now degrades the signal significantly
- Improvements in channel tend to be costly
  - Short-distance optics vs. electrical debate ~15 years old
  - Electronics usually bear the burden

To Make Life Even More Fun...

- Need to achieve all of this within tightly limited power, area budgets
  - With lots of noisy digital blocks nearby
  - And with transistor scaling running out of steam
**Good News**

- Many opportunities for multi-disciplinary innovation
  - Circuits, communications, optimization, E&M, ...

- Will learn how to build (one of) most efficient comm. systems in existence
  - Best designs use only ~0.5-2mW per Gb/s of throughput

- Techniques broadly applicable
  - Even if you end up working on RF, biosensors, data-converters, etc.

**Syllabus**

- Link Environment
  - Channels: physical components, models
  - Link performance evaluation

- Signaling
  - Transmitters, receivers
  - Equalizer types, circuits
  - Adaptation algorithms and implementations

- Timing
  - Clocking and link types
  - Clock and data recovery (CDR)
  - PLLs, DLLs, and phase interpolators

- Support functions
  - Supply regulation
  - Mixed-signal design verification

- Advanced topics (if time permits)