Keep in mind that your goal is to receive the same bits that were sent...

Why Wouldn’t You Get What You Sent?

Most Basic “Link”

Eye Diagrams

With voltage noise

With timing noise

With Both!

Eye Opening - space between 1 and 0

• BER = Bit Error Rate
  • Average # of wrong received bits / total transmitted bits
  • Simplified example: (voltage only)
    \[ BER = \frac{1}{2} \operatorname{erfc} \left( \frac{V_{\text{in,ampl}} - V_{\text{off}}}{\sqrt{2}\sigma_{\text{noise}}} \right) \]
    • BER = 10^{-12}: (V_{\text{in,ampl}} – V_{\text{off}}) = 7\sigma_n
    • BER = 10^{-20}: (V_{\text{in,ampl}} – V_{\text{off}}) = 9.25\sigma_n

What About That “Wire”
“Wire” Models

• ICs: usually use lumped models for wires
  • Capacitance almost always matters
  • Sometimes resistance
  • Less often inductance

• Works because dimensions << \lambda
  • Let’s look at some example \lambda and size numbers for links

Links and Lengths

• Chip to chip on a PCB
  • "Short" and relatively well controlled
  • Packaging usually limits speed
  • Distance: 3-6"
  • Data-rate: 1-12Gb/s
    • Wavelength in free space =
    • Wavelength on PCB (FR4) =

Links and Lengths

• Cables connecting chips on two different PCBs
  • Cables are lossy, but relatively clean if coax
  • Connector transitions usually the bad part
  • Distance: ~0.5m up to ~10’s of m (Ethernet)
  • Data-rate: 1-10Gb/s
    • Wavelength in free space =
    • Wavelength on PCB (FR4) =

Transmission Lines Quick Review

• Delay
• Characteristic Impedance
• Reflections
• Loss

Reflections

• Sources of Reflections : Z - Discontinuities
  • PCB Z mismatch
  • Connector Z mismatch
  • Vias (through) Z mismatch
  • Device parasitics - effective Z mismatch
### Skin Effect
- At high $f$, current crowds along the surface of the conductor
- Skin depth proportional to $f^{-1/2}$
- Model as if skin is $\delta$ thick
- Starts when skin depth equals conductor radius ($\delta_c$)

$$\delta = \left( \pi f \mu \sigma \right)^{1/2}$$

\[ J = \exp \left( - \frac{d}{\delta} \right) \]

![Skin Effect Diagram](image)

### Dielectric Loss
- High frequency signals jiggle molecules in the insulator
  - Insulator absorbs energy
  - Effect is approximately linear with frequency
  - Modeled as conductance term in transmission line equations
  - Dielectric loss often specified in terms of loss tangent
    - Transfer function $= e^{-\eta \tan \delta}$

$$\tan \delta = \frac{G}{\varepsilon_0 C}$$

$$\alpha = \frac{G}{\varepsilon_0 C} = \frac{\pi f \tan \delta \sqrt{LC}}{2}$$

- FR4 $\tan \delta = 0.035$
- Polyimide $0.025$
- GETEK $0.010$
- Teflon $0.001$

![Dielectric Loss Diagram](image)

### Skin + Dielectric Losses
- Skin Loss $\propto \sqrt{f}$
- Dielectric loss $\propto f$: bigger issue at high $f$

- FR4 cheapest – most widely used
- Rogers is most expensive – high-end systems
  - May not matter that much due to surface roughness

![Skin + Dielectric Losses Diagram](image)

### Everything Together: S21
- S21: ratio of received vs. transmitted signals

- PCB traces
- PCB traces & connectors
- PCB traces, connectors & vias
- Entire channel

![Everything Together: S21](image)
Practical PCB Differential Lines

- Differential signaling has nice properties
  - Many sources of noise can be made common-mode
  - Differential impedance raised as \( f(\text{mutuals}) \) between wires
  - Strong mutual L, C can improve immunity

Coupling \(\rightarrow\) Crosstalk...

- “Near-end” xtalk: NEXT (reverse wave)
- “Far-end” xtalk: FEXT (forward wave)
- NEXT in particular can be very destructive
  - Full swing TX vs. attenuated RX signal
  - Good news: can control through design
  - NEXT typically 3-6%, FEXT typically 1-3%

Connectors Particularly Tough

- Tight footprint constraints
- Hard to match pairs and even individual lines
  - May compensate skew on line card
- Also big source of impedance discontinuities
**Skew Within Link**

- Need very tight control to maintain constant % of bit time
- 1% skew on 30" line → 50ps skew
- Half of a bit time at 10Gb/s
- Good news: connectors relatively "short" (~200ps)

**Reflections Revisited**

- Connector-BP transitions

**Minimizing Via Stubs**

- Thinner PCB?
- Better vias?
- All expensive: 1.1-2x

**Reflections Due To Via Stub**

- "Stub": extra piece of T-line hanging off main path
- Usually leads to resonance (notch)
- Especially on thick backplanes, vias are a big culprit

**Summary**

- Packaging, chip connection, etc. can all have an effect...
- Entire conferences dedicated to "signal integrity" (SI)

**Implications**

- Need to know range of channels you will face
- Drives design of the link circuitry
- Start diving into that next lecture
- Don’t be a pure "circuit weenie"
- Simple fixes to channel may go a long way...