Ultra Low Power Design —
The Road to Disappearing Electronics

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Jan M. Rabaey
and the PicoRadio Group
Berkeley Wireless Research Center
Department of EECS, University of California, Berkeley
http://bwrc.eecs.berkeley.edu
Bell’s Law: A New Computer Class Every 10 Years

Meaning in the Device
Meaning in the Connection
Meaning in the Collection

1940’s 2000’s

log (people per computer)

Year

Courtesy: R. Newton
Disappearing Electronics - The “Ambient Intelligence” Concept

- An environment where technology is embedded, hidden in the background
- An environment that is sensitive, adaptive, and responsive to the presence of people and objects
- An environment that augments activities through smart non-explicit assistance
- An environment that preserves security, privacy and trustworthiness while utilizing information when needed and appropriate

Fred Boekhorst, Philips, ISSCC02
Enabled by Technology Advancements

Moore’s law and size

Moore’s law and cost

SOC/SIP enabling true system integration

Ubiquitous wireless as the glue

BWRC
Creating a whole new world of applications

From Monitoring

To Automation
How to Make Electronics Truly Disappear?

From 10’s of cm³ and 10’s to 100’s of mW

To 10’s of mm³ and 10’s of µW
Meso-scale low-cost wireless transceivers for ubiquitous wireless data acquisition that

- are fully integrated
  - Size smaller than 1 cm³
- are dirt cheap ("the Dutch treat")
  - At or below 1$
- minimize power/energy dissipation
  - Limiting power dissipation to 100 µW enables energy scavenging
- and form self-configuring, robust, ad-hoc networks containing 100’s to 1000’s of nodes
What can one do with 1 cm³?
Reference case: the human brain

\[ P_{\text{avg}}(\text{brain}) = 20 \text{ W} \]
(20% of the total dissipation, 2% of the weight),
Power density: \(\sim 15 \text{ mW/cm}^3\)
Nerve cells only 4% of brain volume
Average neuron density: 70 million/cm³
What can one do with 1 cm$^3$?
Perform computations ...

- 300 million 4 input NAND gates (90 nm)
- 7 million “Xilinx gates” (90 nm)
- Assuming 500 MHz clock frequency, 1V Vdd and fanout of 4 and 10% activity:
  - 15 Peta gate-ops/sec @ 45 W
- Reducing supply voltage to 0.2V and clock rate to 10 MHz: 300 Giga gate-ops @ 40 mW
What can one do with 1 cm³?

Energy Storage

<table>
<thead>
<tr>
<th></th>
<th>J/cm³</th>
<th>µW/cm³/year</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micro Fuel cell</td>
<td>3500</td>
<td>110</td>
</tr>
<tr>
<td>Primary battery</td>
<td>2880</td>
<td>90</td>
</tr>
<tr>
<td>Secondary battery</td>
<td>1080</td>
<td>34</td>
</tr>
<tr>
<td>Ultra-capacitor</td>
<td>100</td>
<td>3.2</td>
</tr>
</tbody>
</table>
What can one do with 1 cm$^3$?

**Energy Generation**

<table>
<thead>
<tr>
<th>Source</th>
<th>$\mu W/cm^3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solar (outside)</td>
<td>15,000</td>
</tr>
<tr>
<td>Air flow</td>
<td>380</td>
</tr>
<tr>
<td>Human power</td>
<td>330</td>
</tr>
<tr>
<td>Vibration</td>
<td>200</td>
</tr>
<tr>
<td>Temperature</td>
<td>40</td>
</tr>
<tr>
<td>Pressure Var.</td>
<td>17</td>
</tr>
<tr>
<td>Solar (inside)</td>
<td>10</td>
</tr>
</tbody>
</table>
Towards a sub-100 $\mu W$ Integrated Node

**Some Overall Guidelines**

- Consider ALL components
- Keep it simple!
- Minimize the supply voltage and the ambient currents as much as possible
- Aggressive use of new technologies (RF-MEMS, integrated passives, ...)
- Manufacturability is key
Towards a sub-100 μW Integrated Node

- Simplest possible architecture
- Minimize on-current by aggressive usage of passives
- Minimize supply voltage
- Turned off most of the time / fast turn-on
Low-Power RF: Back to The Future
(Courtesy of Brian Otis)

© 2000 - Direct Conversion
- $f_c = 2$GHz
- $>10000$ active devices
- no off-chip components

© 1949 - superregenerative
- $f_c = 500$MHz
- 2 active devices
- high quality off-chip passives - hand tuning

D. Yee, UCB
The Return of Super-regenerative

- Fully integrated receiver front-end
- Minimizes use of active components – exploits new technologies such as RF-MEMS
- Uses simple non-linear modulation scheme (OOK)
- Down-conversion through non-linearity (diode)

FBAR: Thin-Film Bulk Acoustic Resonator

Operates down to 0.9V!
400 μA when active

OOK modulated (80 dbm signal)

Courtesy: Brian Otis
Energy-efficient Transmitters

LC Power Oscillator to deliver power efficiently and reduce driver power (self-driven)
- Concurrent antenna/power oscillator design
- Power control for optimal radiated power
- Frequency calibration to minimize locking power / FBAR Reference Oscillator

Injection-locked transmitter

TX at 2 mW or less (when on)

Courtesy: Yuen-Hui Chee
Moving forward:
Realizing even lower-power receivers

One option: sub-threshold RF oscillator using integrated LCs

Challenge: How to deal with process variations?

Answer: Use on-chip calibration!

Measured performance @
$V_{dd}=0.5V$ and $I_{dd}=400\mu A$:
$f_{osc} = 1.4 \text{ GHz}; V_{swing} = 125 \text{ mV}$

2.5 ns start-up

Courtesy: Nate Pletcher
Towards a sub-100 μW Integrated Node

- Trade-off between digital and analog
  - Design exploration essential
- Minimize supply voltages < 500 mV
  - Most analog sub-threshold
  - Beware of process variations
### Where analog meets digital

**Mostly Digital?**

- Analog Filter
- ADC
- Synch Detect
- Digital Logic

**Versus Mostly Analog?**

- Slicer
- Synch Detect
- Digital Logic

### The power of exploration...

<table>
<thead>
<tr>
<th></th>
<th>Mostly Analog</th>
<th>Mostly Digital</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Power (uW)</td>
<td>17 (control)</td>
<td>49 (correlate, control)</td>
</tr>
<tr>
<td>Analog Power (uW)</td>
<td>200 (integrators, comparators)</td>
<td>125 (8-bit ADC @ 500KHz)</td>
</tr>
<tr>
<td>Total Power (uW)</td>
<td>217</td>
<td>174</td>
</tr>
<tr>
<td>Header Length (symbs)</td>
<td>23</td>
<td>17</td>
</tr>
</tbody>
</table>

Courtesy Josie Ammer, Yanmei Li, and ASV
Towards a sub-100 µW Integrated Node

- Simplest possible processor
- Dedicated accelerators when needed
- Aggressive power management
- Minimizing supply voltage

Courtesy: Mike Sheets
Call a Plumber… This Thing Leaks!

<table>
<thead>
<tr>
<th>Block</th>
<th>Area (um²)</th>
<th>Logic</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Locationing</td>
<td>337990</td>
<td>39.9</td>
<td></td>
</tr>
<tr>
<td>DW8051</td>
<td>63235</td>
<td>8.2</td>
<td>2880.0</td>
</tr>
<tr>
<td>Interface</td>
<td>6098</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>Neighborlist</td>
<td>21282</td>
<td>2.5</td>
<td>13.5</td>
</tr>
<tr>
<td>Serial</td>
<td>2554</td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td>NetQ</td>
<td>6296</td>
<td>0.7</td>
<td>108.0</td>
</tr>
<tr>
<td>DLL</td>
<td>126846</td>
<td>17.4</td>
<td>13.5</td>
</tr>
<tr>
<td>Supervisor</td>
<td>51094</td>
<td>6.4</td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>76.3</strong></td>
<td><strong>3015.0</strong></td>
<td></td>
</tr>
</tbody>
</table>

Hey buddy, turn down the voltage!
(or turn it off altogether)

64KB SRAM for SW code and data

30X the target power… just in leakage!!

Leakage vs. Supply Voltage

\[ E_{\text{leakage}} \propto V_{dd}^2 \]

Hey buddy, turn down the voltage!
(or turn it off altogether)
The SRAM Data Retention Voltage (DRV)

Lowering the DRV: Sizing and/or correction

Dr. Huifang Qin

4KB SRAM Leakage Current (µA)

Measured DRV range

DRV Spatial Distribution (256*128 Cells)

Courtesy: Huifang Qin
Introducing “Power Domains”

Similar to “clock domains”, but extended to include power-down (really!) and local supply and threshold voltage management.

Who is in charge?

Chip Supervisor (or Chip O/S)
- Initiates power up/down
- Maintains global state and perspective
- Maintains system timers
- Alerts blocks of important events
Moving Forward?  
Ultra-Low Voltage Digital Design

- Aggressive voltage scaling is the premier way of reducing energy dissipation (active and leakage!)
- Design at 250 mV or below is definitely doable
- Sacrifice in performance mitigated by careful threshold manipulation: “Leakage is good for you!”

Challenges:
- Leakage in non-active mode: **power management**
- Wide variation in gate performance due to process variations

(Courtesy: T. Sakurai, T. Kuroda)
The Potential of Adaptive Tuning

Explore circuit and architecture techniques that deal with performance variations (e.g., GALS), are (somewhat) resilient to errors, and dynamically adjust leakage based on activity!
Adaptive Body Biasing

Source: P. Gelsinger (DAC04)
Towards a sub-100 µW Integrated Node

Energy generation and conversion network

- **RF + Antenna**
- **Baseband (mixed-signal)**
- **Clock Generation**
- **Digital Processor(s)**
- **Power Supply**
- **Network Sensors**

**Energy Sources**
- **Energy Source 1 (solar)**
- **Energy Source 2 (vibration, ...)**

**Reservoirs**
- **Reservoir 1 (capacitor)**
- **Reservoir 2 (microbattery)**

**Conversion Networks**
- **Conversion Network 1**
- **Conversion Network 2**

**Electrostatic MEMS vibration converters**

**Microbattery**
Example: On-Chip Voltage Down Converter

Switched-capacitor regulator provides high efficiency (> 80%) at low current levels

Clock frequency adapted to current load

Courtesy: Huifang Qin
Towards a sub-100 μW Integrated Node

MEMS resonator die flips directly onto CMOS for a compact, integrated clock module.

1 μW oscillator
Reliability!

- Narrow-band radios increase sensitivity to fast fading
- Power-cycling deteriorates connectivity
- Low-voltage design opens the door for errors (timing, soft)

But, unreliability is intrinsic to the disappearing electronics concept.

Nodes may appear at will, may move, may fail and (temporarily) run out of energy

The wrong answer: over-design

The right answer: use system-level solutions
Example: Simple radio’s tend to be bad radio’s

Small Change in Path Loss Has Dramatic Impact on Transmission Quality
- Channel is either “good” or “bad”

Solution: use spatial diversity inherently present in ambient intelligence networks

Factor $10^5$ in error rate

Deep fade due to multipath

3 nodes

2 nodes

Data gathered using PicoNode testbed
A System-Level Solution: Opportunistic Routing

- Network specifies forwarding region
- Media-access "randomly" chooses next-hop based on availability and connectivity
- Improves reliability and energy efficiency
Looking forward: Statistical Communication

How to design “NanoNets” — networks of wireless communication nodes that are ~ 1 mm³, consume ~ 1 μW, and cost 1 cent?

- Operate them at very low voltages (< 250 mV)
- Extensive use of passives
- Absolutely no tuning!
- Use statistical networking and density to provide reliability

Integrated GHz LC resonator (N. Pletcher, UCB)

Integrated Finfet NEMS resonator (King, Howe, UCB)
A Statistical Communication Paradigm
“Strength in Numbers”

“Random frequency multi-hopping”
• Information packet traverses from source to destination in a multi-hop fashion.
• Transmitter broadcasts signal to neighboring block on a randomly selected channel.
• Receivers randomly select channel to listen to.

Some Amazing Properties
• Reliable communication over this unreliable platform is indeed possible.
• Even more, reliability improves EXPONENTIALLY with a linear increase in network density.
Summary and Perspectives

• Scaling of technology leads to ever smaller communication and computation nodes
• True smart dust can only be met by ultra low-power design of all components.
• But …cutting on power and energy tends to lead to unreliability.
• An appealing solution: exploit the power of the numbers, and avoid brittleness by embracing randomness
• An opportunity for bold innovation → a first glimpse at the world of nano …

"Research is what I'm doing when I don't know what I'm doing."
– W. Von Braun

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