ON THE SYMBIOTIC NATURE OF INFORMATION TECHNOLOGY AND NEUROSCIENCE

A Few Reflections and Some Examples

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Moore’s Law Hits 50, but It May Not See 60

By Arik Hesseldahl
April 15, 2015 10:11 PM

Moore’s Law turns 50 years old this Sunday. It may not make it to 60.

Since Intel co-founder Gordon Moore first made the observation in a 1965 paper published in Electronics Magazine that the number-crunching capacity of our computers and the number of transistors on silicon chips double roughly every two years, that prediction has underpinned the unrelenting tide of technological progress.
Doomed by Process and Device Limitations

Speed, energy and efficiency plateauing

And Variance/Uncertainty

Energy Minimum Set by Leakage
End of Moore's Law: It's not just about physics

A DARPA director argues that the end of the Moore's Law – which is essentially why you now have a tablet in your hand – could come about because of insurmountable economic challenges.

by Brooke Crothers @mbrookec / August 28, 2013 6:15 AM PDT

An Intel wafer. Chipmakers may find it more difficult to justify the huge costs of developing the next generations of chip technology.

The end of Moore's Law may ultimately be as much about economics as physics, says a DARPA director.

"My thesis here is that it's time to start planning for the end of Moore's Law, and that it's worth pondering how it will end, not just when," Robert Colwell, director of the Microsystems Technology Office at the Defense Advanced Research Projects Agency, told CNET.

"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."


Intel
Doom and Gloom ... Really?
The IT Platform is Already Moving On!

Cyber(bio)physical Systems –
Bridging the physical and the cyber world

A fundamental transformation in engineering

[J. Rabaey, 2008]

[E. Lee, UCB, 2013]
Not Business as Usual

It’s all about Data – Lot’s of it!

Big data:
Making sense of massive amounts of data

The data deluge:
How to survive in a sensor-infused world
Technology Moving on as well ...
Nanotechnology Promise (at the small)

Massive numbers of densely-packed devices
- 3D integrated
- Very broad range of functions: sensing, energy-harvesting and storage, memory, processing and communication

Challenges: Yield, Variability, SNR
Nanotechnology Promise (at the large)

Large area or flexible electronics
- Manufactured by scalable printing
- Very broad range of functions: sensing, energy-harvesting and storage, memory, processing and communication

Challenges: Yield, Variability, SNR
NEED TO REVISIT WHAT WE MEAN BY COMPUTATION

Exciting new applications and platforms
But with their own needs and formidable challenges
Some Contrasting Visions

Main memory

Caches

Processor

Physical computing (-2000)  Biological computing
Some Contrasting Visions

Main memory

Caches

Processor

Physical computing (-2000)

Biological computing
The Neuroscience Promise

2-3 orders more efficient than today’s silicon equivalent (>10^{16} FLOPS with ~20 W)

Robustness in presence of component failure and variations

- Neural response is highly variable ($\sigma/\mu \approx 1$) [Faisal]

Amazing performance with mediocre components

- E.g. sensory pathways– auditory, olfactory, vision, ...

Still marginally understood, let alone “cloned”
This May Change Rapidly

IT, Micro and Nanotechnology to the Rescue
Mapping the Brain

How to dynamically interact (read and write) with large networks of neurons?

A) Electrical

B) Optical

C) Magnetic Resonance

D) Molecular

Also: chemical, acoustic, radioactive, etc

[Courtesy: Marblestone at el, arxiv.org 2013]
Mapping the Brain

Nanoscale “sensor nodes” approaching size of neurons/cells

Matching the power density and potentials of biological systems: a 3.1-nW, 130-mV, 0.023-mm³ pulsed 33-GHz radio transmitter in 32-nm SOI CMOS

J. Choi et al, CICC14

Energy extraction from the biologic battery in the inner ear

P. Mercier et al, Nature12

Stanford Report, May 19, 2014

Stanford engineer invents safe way to transfer energy to medical chips in the body

A. Poon, Stanford
Physical Interface Platforms across Scale and Modality

- **μECoG+BMI**
  - Peter Ledochowitsch / Nathalie Gaudreault
  - Blanche / Maharbiz

- **μECoG for auditory cortex**
  - Peter Ledochowitsch / Raphael Tiefenauer
  - Chang / Maharbiz

- **Scalable Flexible Ultracompliant Nanocables**
  - Peter Ledochowitsch / Raphaël Tiefenauer
  - Blanche / Maharbiz

- **Insertion robotics for ultra-compliant electrodes**
  - Tim Hanson
  - Sabes / Maharbiz

- **High Density Flexible Nanotrodes:**
  - Electrical + Optical
  - Maysam Chamanzarnar
  - Blanche / Maharbiz
A Library of Acquisition, Communication and Power Delivery Components!

Free-floating wireless AP acquisition electrodes [Biederman, Yeager, VLSI12]

Asynchronous 250 nW/channel spike-sorting [Liu, VLSI12]

64 channel remotely powered wireless uECoG [Muller, Le, Ledoschowicz, Li]
Plethora of Neuromodulation Interfaces
Emerging

[Muller et al, 2014]

Just a few ...

[Maysam, Yeager, 2014]
Looking Beyond – Scaling to Thousands and Microns

~50 μm neural dust nodes embedded in cortex or peripheral nervous

Ultrasound outperforms EM in brain tissue

- Ultrasound data/power to dust
- EM link from hub to external transceiver

[DJ Seo et al, Arxiv, June 2013]
First in-Vitro Results (PNS)

[DJ Seo et al, SfN Nov 14]

Successfully reconstructed compound action potential via backscattering
Beyond Mapping and Science

Scalable, Modular, Multi-Scale Interfaces Enable Long-Term Brain Machine Interfaces

[Medtronic PSC-A]

[SubNets OMNI]

[Emotiv]
The Next Step: The Human Intranet

Empowered humans in an Augmented World

Truly novel platforms and application domains enabled by the neuro/IT symbiosis
Back to Computing ...
Opportunity of Neuro-Inspired Computing

• Exploit properties of neural systems
  – Massively parallel and major redundancy
  – Highly variable, non-deterministic, and adaptive
  – Sparse, low resolution, high-dimensional representations

• Combined with features of nanometer CMOS or post-CMOS technology
  – Huge numbers of devices possibly in multiple layers (3D)
  – Intertwined memory and computation
  – Huge variability

To tackle hard cognitive problems addressing sensory data deluge
Functional non-determinism present in most applications related to human-cyber interfaces

- feature extraction
- classification
- synthesis
- recognition
- decision making
- learning, …
The sensory pathway – as nature sees it

Retina
130 Million photoreceptors

Optical nerve:
1 Million fibers
10-100 Mb/sec

Data compression in retina

Massive expansion in V1 and V2

Visual cortex of Macaque monkey

[Courtesy: B. Olshausen, UCB]
The sensory pathway – an engineering interpretation

Sensing
Redundant

Feature extraction
Sparsity

Transformation
Overcomplete/Spatial

Classification
Associative Memory

In-sensor computing

In-memory computing

It is all about data representations!
Choose the right information representation that
- makes computation easy, efficient and robust
- matches the platform!
Embedded Feature Extraction

“In-sensor Processing”

Challenge:
• Address variability and low resolution of mass-produced sensor arrays
• while dealing with limited energy, computational or communication capabilities

Idea: Probabilistic processing embedded in sensor arrays leads to robustness, efficiency and simplicity.
Example:
Inference-based Classifiers Embedded in Sensor Arrays

2-5 weak classifiers based on highly non-ideal (TFT) multipliers achieve performance of ideal SVM

[Courtesy: N. Verma, Princeton]
Example:
Image segmentation using coupled oscillator arrays

Modeled after processes thought to occur in retina

- **What it solves:** finding clusters of strongly connected components in a graph
- **How:** Model as network of phase-coupled oscillators

\[
\frac{d\theta_i}{dt} = \omega_i + \sum_{j=1}^{M} K_{ij} \sin(\theta_j - \theta_i)
\]

[Courtesy: B. Olshausen, UCB]
Hierarchical Knowledge Extraction

“In-memory processing”

Challenge:
• Overcome low SNR, and large variability and uncertainty
• to perform robust decision making and classification
improving both performance and energy efficiency

Idea: Distributed pattern–based hyper-dimensional data representations and arithmetic realized on 3D nanofabrics.
In-Memory Computing?

Evolution in computing architectures
- Increasing parallelism
- Processing moving to memory
- From hot to dark processors
Example: Hyperdimensional (HD) Representations

Representations with dimension “much” (> 10,000) larger than needed to cover space
- Extremely robust against most failure mechanisms and noise
- Purely statistical, thrives on randomness
- Supports full algebra

Superb properties:
- Allow for computation under very low SNR and high variability conditions

Extremely inefficient or even impossible in current 2D platforms

[Ref: P. Kanerva, An Introduction to Computing in Distributed Representation with High-Dimensional Random Vectors, 2009]
Random Indexing/Associative Memory

Example: Identifying Languages

21 languages
1000 sentences/language
Letters only

“Je kunt een scherm verwerken in een bril en een toetsenbord in een polsband, die dan met elkaar communiceren.”

Input Sentence

Random Indexer

10,000 bit random vector

Associative Memory

“dutch”

21,000 10,000D vectors
Stored in Associative Memory

Identified Language

Correct language chosen 97.8% of time
Equally applicable to speech, music, ...

[Courtesy: P. Kanerva, UCB]
Learning (Correlation)

Retrieval (Projection)

Thresholding (Thresholding)
Compelling Fabrics Question

How to efficiently compute: $Y = F(W.X)$ ?
- $Y$ and $X$ are vectors of very large dimension,
- $F$ is an array of non-linear functions,
- $W$ is very sparse (and is either random or learned)

Nature:
- Common neural network

Manufactured nano-fabrics:
- ASIC interconnect fabric

Basic Cerebellum circuit (half of brain neurons)

Addressing the cost of “wires”
Monolithic Random Indexer

Ultra-dense 3D integration of RRAM+CNFET delay cells
Exploit High RRAM + CNFET Variability

[Shulacker, IEDM 14]
Structured Associative Memory

Approximate distributed in-memory computation

Sparse
< 1 % elements switching at any time

Random-Variation Resistant
Law of the numbers

Leakage Resistant
Pulse (event) driven operation
The Roadmap to In-Memory Computing

Micron Hybrid Memory Cube

Samsung 3D NAND Vertical Flash

Stanford true 3D Integration
An exciting time ...

“Brains work with patterns of neural activity that are not readily associated with numbers. The brain’s reliance on high-dimensional distributed representations invites us to study high-dimensional computing, all the more so now that nanotechnology is poised to give us circuits that can scale up to brain-size. To benefit from the technology, we need a theory of computing that matches the technology ...”

P. Kanerva, Berkeley, May 2014.
High-Order Bits ...

- Neuro-inspired and inference-based computational paradigms may be the perfect match to the next generation of nano devices
  - and as such the novel model of computation
- The “known” in neuroscience is still smaller than the “unknown”
  - Information technology a big enabler
- Symbiotic interaction between neuroscience, nano and IT required in either way
- The Upshot: Exciting new “information-centric” applications that will transform society
Still just the top of the Iceberg

‘Biology is hiding secrets well. We just don’t have the right tools to grasp the complexity of what’s going on.’

— Bruno Olshausen

Wired Magazine, 2014
THANK YOU!

MERCI BEAUCOUP!

DANKE SCHÖN!