“Design in the Late-Silicon Age”

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History Proceeds along Ages

Permian  Triassic  Jurassic  Cretaceous  Tertiary  Quarternary

Transitions between era’s most often are marked by mass extinctions
So Does the Electronics Age...

How to avoid the mass extinctions that typically go with transitions between ages?
ASICS on the Road to Extinction (?)

ASIC/ASSP Design Starts

Courtesy R. Camposano, Synopsys
NRE: The Triple Whammy

Mask Cost

Source: Xilinx and Synopsys, Inc
An Era of Fewer, Flexible and Reusable Components

Platforms have taken a firm ground in application areas ranging from wireless, automotive, consumer, media processing, graphics and gaming.
Managing Flexibility and Concurrency

- Dramatically more SOC “programmers” than SOC “designers”

- Easier to create heterogeneous concurrency than to use it!

Need tools and frameworks that support multiple Models-of-Computation in a seamless and expandable way.

The Metropolis Environment (Sangiovanni, UCB)
Watch Out for Paradigm-Shifting Surprises

Structured ASIC or “the return of gate arrays”

- minimized mask cost
- manufacturable
- 50% area overhead for similar performance
- example: VPGA (CMU)

Maskless Lithography

- Eliminates mask cost
- Puts some constraints on design
- No to be expected any day, though

Source: Semiconductor Research Corp.
The Grand Challenges of the Late Silicon Era

(1) Power and Energy

- Puts Bounds on Integration and Performance
- Limits the deployment of “truly ambient electronics”
(2) Uncertainty

- Process Variability puts Synchronous Design Paradigm under Severe Stress

![Graph showing frequency distribution with process variability impact](image_url)
(3) Reliability

- Errors Can and Will Happen
  - Soft errors already a fact
  - Process scaling reduces SNR

TOP OF THE NEWS

SRAM soft errors cause hard network problems

Networking equipment is growing increasingly susceptible to soft errors — nonrecoverable, temporary misfires that can play havoc with things like traffic destinations — as chip and systems designers pile on SRAM to boost performance. MORE
Some Bold Solutions…

(1) Aggressive Voltage Scaling
- Performance through concurrency
- Dynamic adaptation of supply and threshold voltages
- Careful orchestration of system activity

Chandrakasan (MIT):
175 mV DSP (ISSCC 02)

NEEDS SYSTEM-LEVEL APPROACH!
Some Bold Solutions…

(2) Abandon the Purely Synchronous Paradigm

- **Late Binding** – Let the system make the timing decisions
- **Allow occasional timing errors to happen and deal with them!**

NEEDS SYSTEM-LEVEL APPROACH!

Razor (U. Mich): Pseudo-synchronous

Pleiades (Berkeley):
Globally Asynchronous – Locally Synchronous

NEEDS SYSTEM-LEVEL APPROACH!
Some Bold Solutions...

(3) Self-Correcting Architectures

- Designs that detect and correct errors
- Careful use of redundancy and error correction
- Provide reliable computation layered on un-reliable fabrics (as in the communications world)

NEEDS SYSTEM-LEVEL APPROACH!
Transitioning to the Post-Silicon Age

Implementation platforms that work under very low SNR, are non-deterministic, unpredictable and unreliable...
Daunting Perspectives? You bet!

- The search for solutions needs the attention of the brightest minds all over the country and the world. Hence the MARCO Focus Research Center Program!

Bringing together in a collaborative setting the leading minds in design technology for electronics systems.
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**Gigascale System Research Center (GSRC)**

“The design, verification, and test of complex, heterogeneous embedded systems-on-a-chip/package, covering the complete spectrum from system specification to implementation on emerging circuit fabrics.”
Summary

- The semiconductor industry is facing a challenging time. Radically new disruptive solutions are needed.
- The GSRC collaborative model to paradigm-shifting research has proven to be very successful.
- Not Just Research as Usual
- Supporting the transition from the late to the post silicon age

Avoiding Mass-Extinctions Through Preventive Action
Thank you!

http://www.gigascale.org