PROBLEM 1: VTC

In this problem we will analyze the noise margins for a chain of gates. For this problem, $V_{dd} = 2.5V$. Figure 1.b. is a VTC for all three of the inverters in Fig. 1.a. The VTC has four segments, with a transient region between the two flat regions that can be approximated with two second-order curves.

a) Add the voltage sources to Figure 1.a. that you would use for modeling noise coupling to the input and output of gate $M_2$. You should arrange these voltage sources so that they would both impact the noise margin in the same way (i.e., if the voltage source at the input decrease the noise margin, the voltage source at the output should also decrease the noise margin).

Solution:
b) Determine the noise margins for gate $M_2$ when noise couples only to its input.

**Solution:**

![VTC Graph]

To find the noise margin, we need to know $V_{IL}$, $V_{IH}$, $V_{OL}$, and $V_{OH}$ for the inverters. $V_{OH}$ and $V_{OL}$ are clear from the VTC:

$$V_{OH} = 2V, V_{OL} = 0.5V$$

To find $V_{IL}$ and $V_{IH}$, we need to find the unity-gain points on the VTC. To find these points, we’ll need the equations for the VTC in the regions $0.75V \leq V_{in} \leq 1.25V$ and $1.25V \leq V_{in} \leq 1.75V$.

For $0.75V \leq V_{in} \leq 1.25V$, knowing that the curve is second-order, that $V_{out} = 2V$ for $V_{in} = 0.75V$, and that the slope of the VTC is zero at $V_{in} = 0.75V$, we can write:

$$V_{out} = 2 - k_1(V_{in} - 0.75)^2 \quad (0.75V \leq V_{in} \leq 1.25V)$$

To find $k_1$, we just make use of the fact that we know that $V_{out} = 1.5V$ when $V_{in} = 1.25V$:

$$1.5 = 2 - k_1(1.25 - 0.75)^2 \quad \rightarrow \quad k_1 = 2$$

Following essentially the same procedure, for $1.25V \leq V_{in} \leq 1.75V$:

$$V_{out} = 0.5 + 4(V_{in} - 1.75)^2 \quad (1.25V \leq V_{in} \leq 1.75V)$$

Now we can find $V_{IL}$ and $V_{IH}$:
\[
\frac{d\left(2 - 2(V_{in} - 0.75)^2\right)}{dV_{in}} = -1 \rightarrow V_{IL} = 1V \\
\frac{d\left(0.5 + 4(V_{in} - 1.75)^2\right)}{dV_{in}} = -1 \rightarrow V_{IH} = 1.625V
\]

Finally:

\[
\begin{align*}
NM_{HI} &= 2.0V - 1.625V = 0.375V \\
NM_{IL} &= 1.0V - 0.5V = 0.5V
\end{align*}
\]

c) The following piecewise equation describes the VTC of a circuit created by an EE141 student. Is this a digital gate? Why or why not? As part of your answer, you should sketch the VTC of this gate.

\[
V_{out} = \begin{cases} 
2.5V & 0.0V \leq V_{in} < 0.5V \\
2.5V - 4(V_{in} - 0.5V)^2 & 0.5V \leq V_{in} < 1.0V \\
2.5V - V_{in} & 1.0V \leq V_{in} < 1.5V \\
4(V_{in} - 2V)^2 & 1.5V \leq V_{in} < 2.0V \\
0V & 2.0V \leq V_{in} < 2.5V
\end{cases}
\]

**Solution:**

This is indeed a digital gate. Any noise that places the input within the noise margins of this VTC will be attenuated at the output. Note that there is a stable region of the VTC (between $V_{in}=1V$ and $V_{in}=1.5V$) where noise is not attenuated.
However, as long as noise coupling into the gate is less than the noise margin, this will not affect the operation of the system.

**PROBLEM 2: DELAY**

Recall that we have defined the propagation delay $t_p$ as the time between the 50% transition points of the input and output waveforms. In this problem, we will explore how the way you set up a simulation can affect the results you measure. Please turn in a single spice deck that performs the simulations for parts b) through d). You can measure the delays either by using .MEASURE statements in SPICE, or using awaves. If you use awaves however, you should include plots of your waveforms.

![Figure 2.](image)

a) Create a SPICE subcircuit for the inverter shown in Figure 2. Use the following line in your SPICE deck to obtain the correct NMOS and PMOS transistor models:

```plaintext
.LIB '/home/ff/ee141/MODELS/g25.mod' TT
```

To help get you started, we have provided the following example which demonstrates the creation and usage of subcircuits in SPICE. The following input creates an instance named X1 of the MYRC subcircuit, which consists of a 5kΩ resistor and 10fF capacitor in parallel.

```
X1 TOP BOTTOM MYRC

.SUBCKT MYRC A B
R1 A B 5k
C1 A B 10f
.ENDS
```

**Solution:**

```
.SUBCKT inv vdd gnd in out
Mp out in vdd vdd PMOS W=2u L=0.24u
Mn out in gnd gnd NMOS W=1u L=0.24u
.ENDS
```
b) Measure the average propagation delay of an inverter driving four copies of itself. Apply a step input to the first inverter. *Note: Use the M (Multiply) parameter in the subcircuit instantiation to replicate the inverter.*

Solution:

(See part d) for the spice deck)
$t_{pHL} = 67.6\text{ps}, t_{pLH} = 90.0\text{ps}, t_{pavg} = 78.8\text{ps}$

c) Now create a chain of three inverters, each with a fanout of 4. Measure the average propagation delay of the middle inverter in the chain.

Solution:

(See part d) for the spice deck)
$t_{pHL} = 110.4\text{ps}, t_{pLH} = 123.7\text{ps}, t_{pavg} = 117.0\text{ps}$

d) Finally, create a chain of 4 inverters, each with a fanout of 4. Measure the average propagation delay across the second inverter in the chain.
Solution:

\[ t_{pHL} = 109.4\text{ps}, \quad t_{pLH} = 119.9\text{ps}, \quad t_{pavg} = 114.6\text{ps} \]

SPICE Deck:

```
* Homework 2 Problem 2

.LIB '/home/ff/ee141/MODELS/g25.mod' TT

* Inverter SUBCKT Definition
.SUBCKT inv vdd gnd in out
Mp out in vdd vdd PMOS W=2u L=0.24u
Mn out in gnd gnd NMOS W=1u L=0.24u
.ENDS

* Voltage Sources
V1 vdd 0 2.5V
V2 vstep 0 PULSE 0V 2.5V 10p 0.1f 0.1f 10n 20n

* Part B
Xinv1b vdd 0 vstep vout1b inv M=1
Xinv2b vdd 0 vout1b vout2b inv M=4

* Part C
Xinv1c vdd 0 vstep vout1c inv M=1
Xinv2c vdd 0 vout1c vout2c inv M=4
Xinv3c vdd 0 vout2c vout3c inv M=16

* Part D
Xinv1d vdd 0 vstep vout1d inv M=1
Xinv2d vdd 0 vout1d vout2d inv M=4
Xinv3d vdd 0 vout2d vout3d inv M=16
Xinv4d vdd 0 vout3d vout4d inv M=64

* options
.option post=2 nomod

* analysis
.TRAN 1PS 20NS
* Part B Measurement
.MEASURE TRAN tpHLb TRIG V(vstep) VAL=1.25V RISE=1 TARG V(vout1b) VAL=1.25V FALL=1
.MEASURE TRAN tpLHb TRIG V(vstep) VAL=1.25V FALL=1 TARG V(vout1b) VAL=1.25V RISE=1
.MEASURE TRAN tpavgb PARAM='(tpHLb+tpLHb)/2'
* Part C measurement
.MEASURE TRAN tpHLc TRIG V(vout1c) VAL=1.25V RISE=1 TARG V(vout2c) VAL=1.25V FALL=1
.MEASURE TRAN tpLHc TRIG V(vout1c) VAL=1.25V FALL=1 TARG V(vout2c) VAL=1.25V RISE=1
.MEASURE TRAN tpavgc PARAM='(tpHLc+tpLHc)/2'
* Part D measurement
.MEASURE TRAN tpHLd TRIG V(vout1d) VAL=1.25V RISE=1 TARG V(vout2d) VAL=1.25V FALL=1
.MEASURE TRAN tpLHd TRIG V(vout1d) VAL=1.25V FALL=1 TARG V(vout2d) VAL=1.25V RISE=1
```
e) Note that the delays in each one of these cases are different. Which one of these simulations is most realistic?

**Solution:**

Without an infinitely large driver, the slew rate of any real on-chip signal will be finite. Therefore, the simulation setup in part b) (where the propagation delay is measured with a step input) is not realistic.

Notice that there was a small difference between the delays measured in parts c) and d). In part c), the third inverter (which is only there to act as a load for the inverter whose delay we are measuring) has no load. In most real circuits, if a gate wasn’t driving any other gates, there would be no reason to have that gate in the first place. Therefore, the simulation setup in d) is more realistic.

For those who are interested, the main cause of the difference in delay between c) and d) is that the input and output of any CMOS inverter are capacitively coupled to each other. We will discuss this effect further later on in the class.

**PROBLEM 3: ENERGY AND DELAY TRADEOFFS**

As we will discuss in a later class lecture, one model for the propagation delay of a gate is proportional to \( k_{del} \cdot V_{DD} / (V_{DD} - V_T)^2 \), where \( k_{del} \) is a design/technology dependent parameter. In this problem, we will examine the tradeoffs between energy and delay using this model of propagation delay, and our derivation of energy/operation in CMOS gates from Lecture 2. For parts a), b), and c) of this problem, \( V_T = 0.5V \).

a) Use this delay model to plot the energy versus delay of an inverter for multiple values of \( V_{DD} \) from 1V to 2.5V. You should normalize both the energy and delay to the “nominal” case where \( V_{DD} = 2.5V \) (i.e., you do not need to know the value of \( k_{del} \) or the inverter’s load capacitance)

**Solution:**

The energy/operation of a CMOS inverter is \( CV_{DD}^2 \), so the normalized energy is just \( V_{DD}^2/(2.5V)^2 \).
b) Assuming that the capacitance loading the inverter’s output is constant, calculate the amount of energy saved by making the inverter run 20% slower than nominal.

**Solution:**

\[
\frac{k_{del}V_{DDL}}{(V_{DDL} - V_T)^2} = 1.20, \quad V_{DDH} = 2.5V
\]

\[
\frac{V_{DDL}}{(V_{DDH} - V_T)^2} = 1.20 \times 2.5 \div (2.5 - 0.5)^2
\]

\[
\Rightarrow V_{DDL} = 2.22V
\]

A \(V_{DD}\) of 2.22V yields a normalized energy of 0.789. Therefore the energy saved is 21.1%.

c) The energy delay product (EDP) is the product of energy/operation and delay. Create a plot of EDP versus relative delay (the delay and energy should once again be normalized to those at \(V_{DD} = 2.5V\)).
d) As a function of $V_T$, what value of $V_{DD}$ minimizes the EDP of the inverter?

**Solution:**

\[
EDP \propto k_{dd} V_{DD} / \left( V_{DD} - V_T \right)^2 \times C_L V_{DD}^2
\]

\[
\frac{dEDP}{dV_{DD}} = \frac{d \left( V_{DD}^2 \left( V_{DD} - V_T \right)^2 \right)}{dV_{DD}} = 0
\]

\[
\Rightarrow V_{DD} = 3 \cdot V_T
\]