PROBLEM 1: ACTIVITY FACTORS

a) For the circuit below, what are the activity factors of nodes X, Y, Z and Out if 
\( P(A=1) = P(B=1) = P(C=1) = 1/2 \)?

Solution:

For node X and given that the inputs have a 50% probability of being equal to 1, we know that the probability of the output of the NOR gate being a zero is 75%. So:

\[
\alpha_{X0\rightarrow1} = P(X = 0) \times P(X = 1) = \frac{3}{4} \times \frac{1}{4} = \frac{3}{16}
\]

Since an inverter doesn’t really change the signal statistics, the activity factor at its output is the same as its input:

\[
\alpha_{Y0\rightarrow1} = \alpha_{Y1\rightarrow0} = P(X = 1) \times P(X = 0) = \frac{3}{16}
\]

For node Z, we need to know the probability that node Y will be equal to 1 in order to calculate the probability that Z will be high. Node Y is logically equal to A+B, and therefore has a 75% probability of being a 1. Since node C has a 50% probability of being a 1, the output of the NAND gate has a \((3/4)\times(1/2) = 3/8\) probability of being a 0. Therefore:

\[
\alpha_{Z0\rightarrow1} = P(Z = 0) \times P(Z = 1) = \frac{3}{8} \times \frac{5}{8} = \frac{25}{64}
\]

\[
\alpha_{OUT0\rightarrow1} = P(Z = 1) \times P(Z = 0) = \frac{5}{8} \times \frac{3}{8} = \frac{25}{64}
\]
b) Assuming that $P(A=1) = P(B=1) = P(Cin=1) = 1/2$, what are the activity factors of $Cout$ and $Sum$ for the full adder shown below?

![Full Adder Diagram](image)

Solution:

A | B | Cin | Cout | Sum
---|---|-----|------|-----
0 | 0 | 0   | 0    | 0   
0 | 0 | 1   | 0    | 1   
0 | 1 | 0   | 0    | 1   
0 | 1 | 1   | 1    | 0   
1 | 0 | 0   | 0    | 1   
1 | 0 | 1   | 1    | 0   
1 | 1 | 0   | 1    | 0   
1 | 1 | 1   | 1    | 1   

We can use the truth table above to determine the activity factors of both outputs.

$$
\alpha_{Cout0\rightarrow1} = P(Cout = 0) \times P(Cout = 1) = \frac{1}{2} \times \frac{1}{2} = \frac{1}{4}
$$

$$
\alpha_{SUM0\rightarrow1} = P(SUM = 0) \times P(SUM = 1) = \frac{1}{2} \times \frac{1}{2} = \frac{1}{4}
$$

PROBLEM 2: DOMINO LOGIC

a) Design a domino circuit whose output is:

$$
out = \overline{A}B + BC + \overline{C}
$$

Assume we have access to true form of the inputs only (A, B and C). Draw a transistor level schematic. Hint: Can you further simplify the logic equation from what we have given you?

Solution:

Using simple logical equivalences (remember that $X \cdot Y + \overline{Y} = X + \overline{Y}$ ) or a Karnaugh map, the logic equation can be reduced to:
\[ \text{out} = A + B + \overline{C} \]

The schematic is shown below:

It is important to know the underlying constraints on A, B and C; A and B can rise during evaluation, but neither one of them can fall. Similarly, C can fall during evaluation, but it is not allowed to rise.

b) Implement the above logic as a single complex, dynamic gate (with four inputs) followed by an inverter.

**Solution:**
First, the logic can be restructured:
After restructuring the logic we can now implement this logic using a simple complex dynamic gate followed by an inverter:

![Diagram of logic circuit]

**PROBLEM 3: DOMINO SIZING AND DELAY**

Consider part of a domino decoder shown below. Assume $C_L = 40\, \text{fF}$, $C_{in} = 5\, \text{fF}$, $C_D = C_G = 2\, \text{fF/\mu m}$, and signal $A$ arrives before $C_{in}$. 

![Diagram of domino decoder]
a) Find the logical effort of each stage for the evaluation edge (rising edge of WL).

**Solution:**

The logical effort of each of the stages for the evaluation edge is

LE1 = 5/6  
LE2 = 3/3 = 1  
LE3 = 5/6

b) Find WN1, WN2, and WN3 to give minimal delay (make sure to include the effect of 16x branching).

**Solution:**

First, the path effort is calculated, and then the effective fanout per stage:

\[ PE = \left(\frac{5}{6}\right)^2 \cdot \left(\frac{40}{5}\right) \cdot 16 = 88.89 \]

\[ EF = (88.89)^{1/3} = 4.46 \]

Now we can size the gates:

\[ Cin_3 = \frac{40}{4.46} \cdot \frac{5}{6} = 7.47 \text{fF} \quad \text{W}_3 = 0.747 \text{um} \quad \text{and} \quad 4\text{W}_3 = 2.988 \text{um} \]

\[ Cin_2 = \frac{7.47}{4.46} \quad \text{W}_2 = 0.835 \text{um} \]

\[ Cin_1 = 5 \text{fF} \quad \text{W}_1 = 0.5 \text{um} \quad \text{and} \quad 4\text{W}_1 = 2 \text{um} \]

c) Estimate the delay of the path in F04. Include the parasitic delay terms. Recall that 1FO4 is equal to \((4 + \gamma)t_{inv}\).

**Solution:**

\[ 1FO4 = \left(4 + \frac{2\text{fF/um}}{2\text{fF/um}}\right) t_{inv} = 5t_{inv} \]

Delay = \(N \cdot EF \cdot t_{inv} + \sum (P)\)

Since we already know the number of stages (N) and the effective fanout per stage (EF), our main task here is to calculate the parasitic portion of the delay.

For a skewed inverter, the ratio of the skewed inverter’s diffusion capacitance to that of a standard (un-skewed) inverter with the same drive resistance is 5/6. Thus, \(P_{skewed\_inv} = (5/6)t_{inv}\)

For the dynamic NAND gate, assuming that clk goes high before the other inputs transition, the parasitic portion of the delay (i.e., the component of delay that doesn’t depend on the size of the next gate) is:
\[
t_{\text{par_dyn}} = 2R_{sqn} \cdot \frac{L}{W_n^2} \cdot (2W_n^2C_D + W_n^2C_G) + 3R_{sqn} \cdot \frac{L}{W_n^2} \cdot [(4/3)W_n^2C_D]
\]
\[
t_{\text{par_dyn}} = 2R_{sqn} \cdot L \cdot C_G \cdot (2C_D/C_G + 1) + 4R_{sqn} \cdot L \cdot C_G \cdot (C_D/C_G)
\]

Normalizing to \( t_{\text{inv}} = 3R_{sqn} \cdot L \cdot C_G \):

\[
P_{\text{dyn}} = \frac{(4/3)C_D/C_G + (2/3) + (4/3)C_D/C_G}{t_{\text{inv}}} t_{\text{inv}}
\]
\[
P_{\text{dyn}} = \frac{(10/3) t_{\text{inv}}}{t_{\text{inv}}}
\]

Therefore, the total delay of this chain is:

\[
\text{Delay} = (4.46 \cdot 3)t_{\text{inv}} + (5/6 + 5/6 + 10/3)t_{\text{inv}}
\]
\[
= 18.38 \ t_{\text{inv}}
\]
\[
= 18.38 / 5 = 3.676 \text{ FO4}
\]

d) From the standpoint of minimum delay, is this the optimum number of stages? If not, then in theory how many stages would need to be added?

**Solution:**

We know from lecture that we’d like the electrical effort (i.e., capacitive fanout) of our fastest gates to be 4. For the case of domino gates, we can approximate the LE per stage as roughly 0.75. So an electrical fanout of 4 translates into an Effective Fanout of \(0.75 \cdot 4 = 3\).

The PE for the given chain of gates was computed as 88.89. Hence the optimal number of stages for minimum delay = \(\log_3(88.89) \approx 4\) stages. Thus, to achieve the minimum delay we would actually want to use four stages in this domino decoder.