Announcements

- Project phase 3 final report due Monday
  - Project wrap-up discussion next Tuesday?
- Final exam
  - Tues. Dec. 15th, 5-8pm, Location TBD
  - Review session: Mon. Dec. 14th
- HKN surveys end of class today

Binary Multiplication

\[
\begin{array}{cccc}
1 & 0 & 1 & 0 \\
\times & 1 & 0 & 1 \\
\hline
1 & 0 & 1 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
+ & 1 & 0 & 1 & 0 & 1 & 0 \\
\hline
1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 0 \\
\end{array}
\]

The Array Multiplier

Class Material

- Last lecture
  - I/O Design
  - Power Distribution
- Today’s lecture
  - Multipliers
**The M-by-N Array Multiplier: Critical Path**

The critical path for a multipliers includes:
- Critical Path 1
- Critical Path 2
- Critical Path 1 & 2

Critical path:

\[ t_{\text{critical}} = [(M-1) + (N-2)] + [(N-1) - 1] + t_{\text{out}} \]

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**Wallace-Tree Multiplier**

Partial products:
- First stage
- Second stage
- Final adder

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**Carry-Save Multiplier**

The Carry-Save Multiplier uses a Vector Merging Adder:

\[ t_{\text{carry}} = t_{\text{out}} + (N-1) - t_{\text{carry}} + t_{\text{entry}} \]

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**Multiplier Floorplan**

- HA Multiplier Cell
- FA Multiplier Cell
- Vector Merging Cell

X and Y signals are broadcasted through the complete array.

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**Multipliers – Summary**

- Optimization constraints different than in binary adder
  - Once again:
    - Need to identify critical path
    - Find ways to use parallelism to reduce it
  - Other possible techniques
    - Logarithmic versus linear (Wallace Tree Mult)
    - Data encoding (Booth)
    - Pipelining

First glimpse at system level optimization