Logic Gates

At the end of this laboratory exercise, you should be able to:

- Create schematics and layouts of NAND and NOR gates using Virtuoso Layout XL.
- Design an XOR gate from NAND gates, NOR gates and inverters.
- Simulate the extracted XOR gate.

Deliverables for this laboratory exercise: **Due at the end of the laboratory session**

- Printout of the simulation results for an XOR gate using NAND gates, NOR gates and inverters.
- Printout of the XOR gate schematic and layout.

I. Creating the NOR Gate Schematic

Create a 2-input CMOS NOR gate as shown below. Create a symbol for this gate as well.

Before proceeding with the layout of this gate, we should first verify whether this gate functions properly in SPICE
(This will check whether the schematic we’ve constructed behaves like a NOR gate). To do this, you can create a
SPICE netlist directly from the schematic cellview in the same way you did with the

\[
\begin{align*}
W_n &= 120\text{nm} \\
W_p &= 480\text{nm}
\end{align*}
\]

Note that the labels will automatically be connected to pins with the same names.
extracted cellview
(but without first having to create a layout view, extracting it, and then simulating it).

In your schematic cellview, open Tools->Analog Environment and from here go to Setup->Simulator/Directory/Host and change the simulator to hspiceD and enter a path to save your netlist.

Finally, select Simulation->Netlist->Create to create a SPICE netlist.

Note: these steps are exactly the same as those you did to do post-layout simulation when you created a SPICE netlist from your extracted cellview. We’re just doing this from the schematic cellview to make sure that our schematic is correct and behaves as it should. (If we didn’t and made a mistake in the schematic, DRC and LVS may still pass but when doing post-layout simulations, our gate would behave incorrectly and we’d have to repeat all the steps of re-creating the schematic and layout to fix the mistake)

Now, create a new SPICE netlist and copy & paste the transistor instantiations from the step above. Add stimuli to the newly-created netlist and test the complete functionality of your NOR gate. (Hint: There are 2 inputs and 2 possibilities for each input, so look at OUT for all 4 possibilities)

II. Creating the NOR Gate Layout

Create a layout view of your NOR gate and click on Tools → Layout XL in the layout editor’s menu bar to enter the Virtuoso XL editing mode. To transfer the schematic instances and pins, click on Connectivity → Update → Components and Nets from the Virtuoso XL menu bar. The Layout Generation Options window will appear.

This is quite a complex form so read the steps carefully.

1. Make sure that the I/O pins, Instances and Boundary boxes are selected.
2. Set the default pin type to Symbolic and the Layer/Master option to Metal1_T.
3. Click Apply. This should update the pin table.
4. Set the Pin Label Shape to Label.
5. Set the Boundary Height to 3.6 microns.
6. Click on the Pin Label Options… to open the Set Pin Label Text Style window (shown below).
7. Make sure the options are the same as the one below, then click OK.
8. In the Layout Generation Options
window, click **OK**.
Upon clicking OK in the *Layout Generation Options* window, the devices and pins in your schematic will be instantiated as shown below.

Create two 0.6 micron supply rails (one for *vdd* and one for *gnd*) similar to the one you made for the inverter. Move the *vdd* and *gnd* pins to these rails.

Afterwards, create an **NWELL** rectangle covering the upper half of the cell boundary.
Next, add **M1_NWELL** and **M1_PSUB** contacts on the appropriate supply rail. Lastly, place all the transistors and pins inside the cell boundary.

Your layout should look similar to the one below.

Notice that while moving the pins or transistors, you will see the interconnect information obtained from the schematic. This will serve as a guide in selecting the best placement of the transistors and pins relative to each other.

An interesting function of the Virtuoso XL layout editor is that when two transistors are connected in series, and you place them together, the middle connection will be removed (if no contact is needed there).

Place the transistors and pins and use paths to connect them, similar to what you did in previous laboratory exercises. Your layout should look similar to the one below.

Remember to check properties of the **vdd** and **gnd** pins for the correct **Net Expression Property** and **Default** entries.

Note the series PMOS transistors have no contact.
Run DRC, circuit extraction and LVS on your NOR gate layout and make sure that there are no errors.

III. Creating the NAND Gate Schematic and Layout

Create a 2-input CMOS NAND gate using the same steps as for the NOR gate and test its functionality using SPICE.
You will start with a schematic similar to the one below with $W_n = 240$nm and $W_p = 240$nm.

$W_n = 240$nm
$W_p = 240$nm

Note that the labels will automatically be connected to pins with the same names.
Again use the same steps you did with the NOR gate to obtain a layout similar to the one below.

Remember to check properties of the \textit{vdd} and \textit{gnd} pins for the correct \textbf{Net Expression Property} and \textbf{Default} entries.

Note the series NMOS transistors have no contact between them.

Again, run DRC, circuit extraction and LVS on the NAND gate and make sure that there are no errors.

\textbf{IV. Designing the XOR Gate}
An XOR gate has the following truth table:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Using the CMOS gates you have already created (the inverter and the NAND and NOR gates), design an XOR gate. First, create a schematic of your XOR gate as well as a symbol for it.

Verify the functionality of your XOR gate schematic by simulating it in SPICE. The inputs to this XOR gate should be driven by unit inverters and the output should be loaded by four unit-sized inverters.

To make this easier, you can create a new schematic and instantiate your XOR gate and inverters and place them as shown below and then create a SPICE netlist of it from your schematic cellview. (You don’t need to add the power supplies as shown below since you can do this in SPICE directly)

Note: each input of the XOR is being driven by unit-sized inverters.

Also note: the output of the XOR gate is being driven by 4 unit-sized inverters (FO4).

After verifying that your schematic is working, create the layout using Virtuoso XL. Again, the layout tool will instantiate all the devices and pins you have instantiated in the schematic.
IMPORTANT: When creating the XOR layout, uncheck the Boundary option in the Layout Generation section of the Layout Generation Options window.

Notice that all the gates we laid out had the same height. This will make the layout very regular. A typical sample layout is shown below. Note that the cells power rails and N-wells are automatically aligned (due to our careful layout strategy).

You can use all the metal layers available to you for routing and you can place the input and output pins anywhere.

You can route outside the vdd and gnd rails if needed.

After completing your layout, run DRC, circuit extraction and LVS. Make sure that there are no errors.

To be submitted:
1. Printout of the simulation results from SPICE for the XOR gate using NAND gates, NOR gates and inverters.
2. Printout of the XOR gate schematic and layout.

End of Lab.