1. Suppose you are a technical director at a video processor company. For the next generation product, you find a choice to make between two fabrication processes. Following table summarizes the main differences between the processes. Due to the current recession, your marketing department reports that expected sale of this product is somewhere between 100,000 to 500,000 pieces. Which process would you choose based on cost considerations? (15 pts)

<table>
<thead>
<tr>
<th>Process</th>
<th>65nm CMOS</th>
<th>90nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost of Mask Set</td>
<td>$3,000,000</td>
<td>$800,000</td>
</tr>
<tr>
<td>Die Size</td>
<td>1.5cm²</td>
<td>2cm²</td>
</tr>
<tr>
<td>Wafer Size</td>
<td>12”</td>
<td>8”</td>
</tr>
<tr>
<td>Yield</td>
<td>78%</td>
<td>85%</td>
</tr>
<tr>
<td>Cost of Wafer</td>
<td>$2,000</td>
<td>$1,200</td>
</tr>
<tr>
<td>Test Cost</td>
<td>$0.68/die</td>
<td></td>
</tr>
<tr>
<td>Packaging Cost</td>
<td>$0.40/chip</td>
<td></td>
</tr>
<tr>
<td>Final Test Yield</td>
<td>95%</td>
<td></td>
</tr>
</tbody>
</table>

Table 1 Cost related parameters of two process candidates.

Solution:

Number of dies per wafer is

$$N_d = \frac{\pi \times \left( \frac{D}{2} \right)^2}{A_{die}} = \frac{\pi \times D}{\sqrt{2} \times A_{die}}$$

where D is the wafer diameter, and A_{die} is the die area. Die cost is

$$C_d = \frac{C_{wafer}}{N_d \times Y}$$

where C_{wafer} is the wafer cost and Y is the yield. Variable cost is

$$C_v = \frac{C_d + C_{test} + C_{pkg}}{Y_{final}}$$

where C_{test} is the test cost, C_{pkg} is the packaging cost and Y_{final} is the final test yield.

Based on above equations, following table compares related parameters between the processes:

<table>
<thead>
<tr>
<th>Process</th>
<th>65nm CMOS</th>
<th>90nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Dies per Wafer</td>
<td>416</td>
<td>125</td>
</tr>
<tr>
<td>Die Cost</td>
<td>$6.16</td>
<td>$11.29</td>
</tr>
<tr>
<td>Variable Cost</td>
<td>$7.62</td>
<td>$13.02</td>
</tr>
<tr>
<td>Fixed Cost per Die</td>
<td>$3,000,000/N</td>
<td>$800,000/N</td>
</tr>
</tbody>
</table>
where $N$ is the number of chips to be sold.

At $N>407,407$, it is more economical to fabricate it in 65nm CMOS. This falls within the range of estimated sale volume. It makes sense to argue for the 90nm technology, because the average of estimation is 300,000, lower than the break-even point. But you can also argue that economy will become better, the marketing people are playing conservative…

2. A hypothetic inverter has the following Voltage Transfer Characteristic (VTC).

![VTC of a hypothetic inverter](image)

(1) What are the noise margins $N_{\text{MH}}$ and $N_{\text{ML}}$? (10 pts)

(2) Inverters have this interesting property that if an odd number of inverters are placed in cascade, they behave like a single inverter. Assume 3 such inverters are cascaded as shown in Figure 2. What are the $N_{\text{MH}}$ and $N_{\text{ML}}$ of the composite inverter? Do you notice difference in VTC between part (1) and (2)? Difference in noise margins? Briefly explain why there is or isn’t difference. (15 pts)

![Cascading 3 unit inverters becomes one composite inverter](image)

**Solution:**

(1) $V_{\text{OH}}=5\text{V}$, $V_{\text{OL}}=0\text{V}$, $V_{\text{IH}}=3\text{V}$, $V_{\text{IL}}=2\text{V}$. Therefore: $N_{\text{MH}}=2\text{V}$, $N_{\text{ML}}=2\text{V}$. 
(2) VTC of an inverter describes its DC operating points. DC operating points of the composite inverter can be found by first mirroring the original VTC over the x=y axis then recursively pairing output with input. Following figure illustrates the process. For $V_{in}=2V$, the original VTC yields output of the first inverter to be 4V, which becomes the input to the second inverter. From the mirrored VTC, output of the second inverter is $\frac{1}{2}V$, which in turn is the input to the third inverter. Finally the original VTC shows $4\frac{3}{4}V$ as output of the third inverter. This makes the pair of $(V_{in}=2V, V_{out}=4\frac{3}{4}V)$. Note that both VTC curves are piece-wise linear. One therefore only needs to perform the recursive pairing at selective points.

Following above process, one can show the VTC of the composite inverter as follows

where $V_{OH}=5V, V_{OL}=0V, V_{IH}=2.67V, V_{IL}=2.33V$. Therefore: $NM_{H}=2.33V, NM_{L}=2.33V$.

There is difference in both VTC and in noise margin. Noise margin improves because of the regenerative property of the inverter VTC – when more inverters connected in cascade, the overall VTC resembles more that of an ideal inverter.
3. Following schematic exemplifies a (heavily) simplified clock distribution network. The first inverter is of minimum size ($1\times$). Input capacitance of a minimum-size inverter is $C$. Also assume $\gamma = 1$.

![Clock Distribution Network Diagram]

Figure 3 Two-path clock distribution.

(1) Suppose that the top path with $20C$ loading is the critical path, which you care the most about its propagation delay. Size the rest of the inverters in Fig. 3 to minimize that delay. Feel free to say “don’t care” if there are inverters that you don’t care about their sizing. (10 pts)

(2) Repeat part (1), assuming that the bottom path with $100C$ is the critical path instead. (5 pts)

(3) Finally assume that both paths are equally critical. Size the inverters so that the average of the two delays is minimized. (15 pts)

Solution:

(1) Size of the four un-sized inverters is labeled as following. For the first case where you only care the delay of the top path, $m_1$ should apparently be minimized to reduce its loading on the other path. Therefore:

$m_1 = 1$

Propagation delay of the top path is then

$$t = t_{p0} \times \left(1 + \frac{n+1}{1} + 1 + \frac{20}{n}\right)$$

$$\frac{\partial t}{\partial n} = t_{p0} \times \left(1 - \frac{20}{n^2}\right) = 0 \Rightarrow n = \sqrt{20}$$

$m_2$ and $m_3$ are apparently “don’t-care”.
(2) Similar to part (1),

\[ n = 1 \]

Propagation delay of the bottom path is then

\[ t = t_{p0} \times \left( 1 + \frac{m_1 + 1}{1} + 1 + \frac{m_2}{m_1} + 1 + \frac{m_3}{m_2} + 1 + \frac{100}{m_3} \right) \]

\[ \frac{\partial t}{\partial m_1} = \frac{\partial t}{\partial m_2} = \frac{\partial t}{\partial m_3} = 0 \Rightarrow m_1 = m_2 = m_3 = \frac{100}{m_3} \]

Therefore

\[ m_1 = (100)^{\frac{1}{4}}, \quad m_2 = (100)^{\frac{1}{2}}, \quad m_3 = (100)^{\frac{3}{4}} \]

(3) Finally, express the average delay of top and bottom paths in terms of \( n \), and \( m_1\text{--}3 \):

\[ t = \frac{t_{p0}}{2} \times \left( 6 + 2 \times \frac{n + m_1}{1} + \frac{20}{n} + \frac{m_2}{m_1} + \frac{m_3}{m_2} + \frac{100}{m_3} \right) \]

\[ \frac{\partial t}{\partial n} = \frac{\partial t}{\partial m_1} = \frac{\partial t}{\partial m_2} = \frac{\partial t}{\partial m_3} = 0 \]

Therefore

\[ n = \sqrt{10}, \quad m_1 = (200)^{\frac{1}{4}}, \quad m_2 = (200)^{\frac{1}{2}}, \quad m_3 = (200)^{\frac{3}{4}} \]