1. We sometimes design the inverter to favor one transition. Fig 1 shows two examples with unequal rising and falling delays.

![Figure 1 Skewed inverters.](image)

(1) Calculate the logical effort of the skewed inverters shown in Fig. 1 for both rising and falling output transitions. Which inverter does favor rising output transition? Why? (10 pts)

(2) Suppose the skewed inverters shown in Fig. 1 are included in your digital cell library. Choose and design the inverter m1, m2, and m3 to minimize the delay \( T_d \) for the low-to-high input transition, as shown in Fig. 2. Calculate the delay \( T_d \) and the corresponding delay for the high-to-low input transition. (15 pts)

**Solution:**

(1) For skewed inverter (a):

Logical effort for the rising output transition \( = (2 \times 2) / 3 = 4 / 3 \)

Logical effort for the falling output transition \( = (1 \times 2) / 3 = 2 / 3 \)

For skewed inverter (b):
Logical effort for the rising output transition = \((1 \times 2.5)/3 = 5/6\)

Logical effort for the falling output transition = \((2 \times 2.5)/3 = 5/3\)

Skewed inverter (b) has the smaller logical effort for the rising output transition and therefore favors rising output transition.

(2) For the low-to-high input transition, the output of m1 is pulled high, the output of m2 is pulled low, and the output of m3 is pulled high. As a result, we can choose inverter (b) as the second stage, inverter (a) as the third stage, and inverter (b) as the final stage to minimize \(T_d\).

\[
G = 1 \times \frac{5}{6} \times \frac{2}{3} \times \frac{5}{6} = \frac{25}{54}
\]

\[B = 1\]

\[F = 1350\]

\[h = \sqrt[4]{GBF} = \sqrt[4]{\frac{25 \times 1350}{54}} = 5\]

\[f_1 = \frac{h}{g_1} = \frac{5}{1} = 5, \quad f_2 = \frac{h}{g_2} = \frac{5}{\frac{5}{6}} = 6, \quad f_3 = \frac{h}{g_3} = \frac{5}{\frac{2}{3}} = 7.5, \quad f_4 = \frac{h}{g_4} = \frac{5}{\frac{5}{6}} = 6\]

Sizing of gates accordingly:
(Note: I use the same definition in the lecture note. Size 2 gate has twice the input capacitance of a unit inverter)

\[s = 1, \quad m_1 = f_1 = 5, \quad m_2 = f_1 f_2 = 5 \times 6 = 30, \quad m_3 = f_1 f_2 f_3 = 5 \times 6 \times 7.5 = 225\]

\[\frac{T_{dh}}{t_{p_0}} = \sum \left( p_i + \frac{f_i g_i}{\gamma} \right) = \left(1 + \frac{2.5}{3} + \frac{2.5}{3} + \frac{2.5}{3}\right) + \frac{1}{\gamma} \left(5 + 5 + 5 + 5\right) = \frac{3}{3} + \frac{20}{\gamma}\]

For the high-to-low input transition:

\[\frac{T_{dh}}{t_{p_0}} = \sum \left( p_i + \frac{f_i g_i}{\gamma} \right) = \left(1 + \frac{5}{3} + \frac{4}{3} + \frac{5}{3}\right) + \frac{1}{\gamma} \left(5 + 6 \times \frac{5}{3} + 7.5 \times \frac{4}{3} + 6 \times \frac{5}{3}\right) = \frac{5}{3} + \frac{35}{\gamma}\]

2. Following schematic implements the logic equation of \((A+B+C+D)\). The four inverters connected to inputs are minimum sized.
If $C_{load}$ is $25xC_{\text{gmin}}$, where $C_{\text{gmin}}$ is the gate capacitance of a minimum-size inverter. Size the NAND, NOR and INV gates to minimize the propagation delay from input to output. (10 pts)

(2) Repeat part (1) if $C_{load}$ is $1xC_{\text{gmin}}$. Be reminded that the input inverters are already minimum sized. Subsequent gates therefore cannot be smaller than unit size. (10 pts)

(3) Can you design another circuit that implements the same logic but has shorter propagation delay for the case of $C_{load}=1xC_{\text{gmin}}$? The four input inverters come from the I/O interface design. They can neither be replaced nor be resized. (10 pts)

Solution:

(1) $G = 1 \times \frac{4}{3} \times \frac{5}{3} \times 1 = \frac{20}{9}$

$B = 1$

$F = 25$

$h = \frac{4 \sqrt{GBF}}{9} = \frac{4 \sqrt{20 \times 25}}{9} = 2.73$

$f_1 = \frac{h}{g_1} = \frac{2.73}{1} = 2.73$, $f_2 = \frac{h}{g_2} = \frac{2.73}{4} = 2.0$, $f_3 = \frac{h}{g_3} = \frac{2.73}{5} = 1.6$,

$f_4 = \frac{h}{g_4} = \frac{2.73}{1} = 2.73$

Sizing of gates accordingly:

$s_1 = 1$, $s_2 = \frac{f_1 g_1}{g_2} = \frac{2.73 \times 1}{4} = 2.0$, $s_3 = \frac{f_1 f_2 g_1}{g_3} = \frac{2.73 \times 2.0}{5} = 3.3$,

$s_4 = \frac{f_1 f_2 f_3 g_1}{g_4} = \frac{2.73 \times 2.0 \times 1.6}{1} = 8.7$

(Above sizing is based on unit-size NAND and NOR gates that have equal resistance as a unit-size inverter. If unit-size NAND and NOR gates are sized with equal input,
capacitance as a unit-size inverter, sizing should then be: \( s_1 = 1 \), \( s_2 = 2.7 \), \( s_3 = 5.5 \) and \( s_4 = 8.7 \).)

(2) Using the same approach as in (1):

\[
h = \sqrt[3]{GBF} = \sqrt[3]{\frac{20 \times 1}{9}} = 1.22
\]

\[
s_2 = \frac{f_2 g_2}{g_2} = \frac{1.2 \times 1}{4} = 0.9 < 1, \text{ this is impractical because a gate cannot be smaller than unit size } \Rightarrow s_3 = 1
\]

(You get full credits too if you argue that the NAND gate can be sized down to 0.5x, because the minimum transistor width in a unit-size NAND gate is 2. This apparently does not apply to an NOR gate.)

Now apply logical effort analysis to the 3-stage circuit starting with NAND since its size has been fixed.

\[
h = \sqrt[3]{GBF} = \sqrt[3]{\frac{20 \times 1}{9}} = 1.3
\]

\[
f_2 = \frac{h}{g_2} = \frac{1.3}{4} = 0.98, \quad f_3 = \frac{h}{g_3} = \frac{1.3}{5} = 0.78, \quad f_4 = \frac{h}{g_4} = 1.3
\]

Therefore,

\[
s_2 = 1, \quad s_3 = \frac{f_2 g_2}{g_3} = \frac{1.3}{5} = 0.78 < 1. \text{ Again this is impractical } \Rightarrow s_3 = 1
\]

Finally apply logical effort analysis to the 2-stage circuit starting with NOR.

\[
G = \frac{5}{3} \times 1 = \frac{5}{3}
\]

\[
h = \sqrt[3]{GBF} = \sqrt[3]{\frac{5 \times 1}{3}} = 1.3
\]

\[
f_3 = \frac{h}{g_3} = \frac{1.3}{5} = 0.78, \quad f_4 = \frac{h}{g_4} = 1.3
\]

\[
s_3 = 1, \quad s_4 = \frac{f_3 g_3}{g_4} = \frac{1.3}{1} = 1.3
\]

Final sizing schematic:
(Again above sizing is based on unit-size NAND and NOR gates that have equal resistance as a unit-size inverter.)

(3) Actual fan-out in above schematic:

\[ f_4 = 1.3, \quad f_3 = \frac{s_4 g_4}{g_3} = \frac{1.3 \times 1}{\frac{5}{3}} = 0.78, \quad f_2 = \frac{s_4 g_3}{g_2} = \frac{1 \times \frac{5}{3}}{\frac{4}{3}} = 1.25, \]

\[ f_1 = \frac{s_3 g_2}{g_1} = \frac{1 \times \frac{4}{3}}{1} = 1.33 \]

Total propagation delay is

\[ \frac{t}{t_{p0}} = \sum \left( p_i + \frac{f_i g_i}{\gamma} \right) = \left( 1 + 2 + 2 + 1 \right) + \frac{1}{\gamma} \left( 1.33 + 1.25 \times \frac{4}{3} + 0.78 \times \frac{5}{3} + 1.3 \right) = 6 + \frac{5.6}{\gamma} \]

By rearranging the circuit to the following, propagation delay can be reduced (there are other options such as using 4-input NOR):

Total propagation delay is:

\[ \frac{t}{t_{p0}} = \sum \left( p_i + \frac{f_i g_i}{\gamma} \right) = \left( 1 + 2 + 2 + 1 \right) + \frac{1}{\gamma} \left( 1.33 + 0.9 \times \frac{4}{3} + 1.21 + 0.9 \times \frac{4}{3} \right) = 6 + \frac{4.9}{\gamma} \]

3. Following schematic exemplifies a clock distribution network. The first inverter is of minimum size (1×). Input capacitance of a minimum-size inverter is C. Also assume γ = 1.
(1) Size the inverter m1 and m2 for the minimum delay. (5 pts)
(2) Assume all inverters share the same supply Vdd. What is the total energy drawn from the supply when the input switches from 0 to Vdd? What is the total energy dissipated as heat? (10 pts)

Solution:

(1) For the first two stages:
\[ G = 1 \times 1 = 1 \]
\[ B = 1 \]
\[ F = 16 \]
\[ h = \frac{3}{\sqrt[3]{GBF}} = \frac{3}{\sqrt[3]{16}} = 4 \]
\[ \Rightarrow m1 = 4 \times 1 = 4 \]

For the last two stages:
\[ G = 1 \times 1 = 1 \]
\[ B = 2 \]
\[ F = 8 \]
\[ h = \frac{3}{\sqrt[3]{GBF}} = \frac{3}{\sqrt[3]{16}} = 4 \]
\[ \Rightarrow m2 = 4 \times 4 / 2 = 8 \]

(2) The total energy drawn from the supply when the input switches from 0 to Vdd is:
\[ E_{\text{Vdd}} = (C_{\text{int,stage2}} + C_{\text{load,stage2}} + C_{\text{gate,stage2}} + 2C_{\text{int,stage4}} + 2C_{\text{load,stage4}}) \cdot Vdd^2 \]
\[ \Rightarrow E_{\text{Vdd}} = (4C + 12C + 4C + 16C + 64C) \cdot Vdd^2 = 100CVdd^2 \]

The total energy dissipated as heat is:
\[ E_{\text{heat}} = 0.5C_{\text{total}} \cdot Vdd^2 \]
\[ \Rightarrow E_{\text{heat}} = 0.5(C + 8C + 12C + 8C + 32C + 64C) \cdot Vdd^2 = 62.5CVdd^2 \]