1. Given the RC network below:

![RC Network Diagram]

Figure 1 RC network.

(1) Calculate the Elmore delay from In to Out1 and from In to Out2. Which one is critical path? (10 pts)

(2) Assume $R = 100\, \Omega$ and $C = 10\, \text{fF}$. Calculate the Elmore delay of the critical path you find in part (1) and verify the result using Spectre. (10 pts)
2. In the following problem, we will calculate the delay of a NAND2 gate by using two approaches we have learned, logical effort and Elmore delay. The NMOS and PMOS can be modeled as a RC network shown below when the transistor is “ON”. When the transistor is “OFF”, we use the same model except now the transistor has an infinite off-resistance. Assume $\gamma = 1$.

![Figure 2 A NAND2 gate and NMOS and PMOS transistor models.](image)

(1) Calculate the $T_{pLH}$ and $T_{pHL}$ of a NAND2 gate shown above using logical effort. (5 pts)
(2) Calculate the $T_{pLH}$ and $T_{pHL}$ of a NAND2 gate shown above using Elmore delay. Do you get different answers in delay between part (1) and (2)? Briefly explain why there is or isn’t difference. (15 pts)