1. In this problem, we will extract fundamental information from the simulation results to build an approximate transistor model for use in hand calculations. Use the same transistor model in HW1 for your simulation.

(1) First generate the family of \( I_D - V_{DS} \) curves for an NMOS transistor (see Lecture #10 slides 30 and 31 for examples) with the following parameters. (5 pts)

- \( W/L = 0.12 \mu m/0.1 \mu m \)
- \( V_{DS} = \) from 0V to 1V
- \( V_{GS} = 0V, 0.2V, 0.4V, 0.6V, 0.8V, \) and 1V
- \( V_{BS} = 0V \)

(2) Suppose we already have some model information from our device friend regarding this technology: \( 0.1V < V_{T0} < 0.2V, 0.3V < V_{DSAT} < 0.4V \).

Complete the \( I_D \) column by simulation and determine the operation region of the NMOS transistor based on the model information you have. (5 pts)

<table>
<thead>
<tr>
<th>Experiment</th>
<th>( V_{GS} )</th>
<th>( V_{DS} )</th>
<th>( V_{BS} )</th>
<th>( I_D )</th>
<th>Operation Region</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1V</td>
<td>0.6V</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1V</td>
<td>0.2V</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>0.4V</td>
<td>0.8V</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>0.4V</td>
<td>0.6V</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>0.2V</td>
<td>0.6V</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(3) Based on the table in part (2), determine the following model parameters: \( V_{T0}, k_n, \lambda, \) and \( V_{DSAT} \). (20 pts)
(1) Solution:

(2) Experiment | $V_{GS}$ | $V_{DS}$ | $V_{BS}$ | $I_D$ | Operation Region
---|---|---|---|---|---
1 | 1V | 0.6V | 0 | 69.99uA | Velocity Saturation
2 | 1V | 0.2V | 0 | 40.64uA | Linear
3 | 0.4V | 0.8V | 0 | 12.93uA | Saturation
4 | 0.4V | 0.6V | 0 | 10.51uA | Saturation
5 | 0.2V | 0.6V | 0 | 0.71uA | Saturation

(3) To calculate $V_{TO}$, use the data from Exp. 4 and 5 and the following equation twice:

$$I_D = k' \frac{W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$\Rightarrow V_T = 0.13V$$

To calculate $\lambda$, use the data from Exp. 3 and 4 and the following equation twice:

$$I_D = k' \frac{W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$\Rightarrow \lambda = 3.71V^{-1}$$

To calculate $k_n$, use the data from Exp. 4 and the following equation:

$$I_D = k' \frac{W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$
To calculate $V_{DSAT}$, use the data from Exp. 1 and the following equation:

$$I_D = k' \frac{W}{L} [(V_{GS} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2}](1 + \lambda V_{DS})$$

$$\Rightarrow V_{DSAT} = 0.35V$$

2. In this problem, you are asked to calculate various capacitances of an inverter and use this information to estimate propagation delay when the wire delay is significant.

![Figure 1](image1.png)

**Figure 1** Equivalent capacitance model in a unit size inverter chain.

![Figure 2](image2.png)

**Figure 2** FO4 inverter chain with a long wire connecting the 1st and 2nd stages.

(1) Use the following technology parameters from the textbook to calculate the equivalent $C_{intLH}$, $C_{intHL}$, $C_{givnLH}$, and $C_{givnHL}$ of a unit size inverter (NMOS: $0.3\mu m/0.25\mu m$ and PMOS $0.6\mu m/0.25\mu m$) in an inverter chain shown in Fig. 1. Assume the supply equals 2.5V and the inverter switches at VDD/2. Also assume for a unit size inverter: $A_{Sn}=AD_{S}=0.25\mu m^2$, $PS_{n}=PD_{n}=1.5\mu m$, $A_{Sp}=AD_{P}=0.3\mu m^2$, $PS_{p}=PD_{p}=3\mu m$. (20 pts)

NMOS:

- $C_{ox} = 6 \, fF/\mu m^2$
- $C_{o} = 0.31 \, fF/\mu m$
- $C_{j} = 2 \, fF/\mu m^2$
- $m_{j} = 0.5$
- $C_{jsw} = 0.28 \, fF/\mu m$
- $m_{jsw} = 0.44$
- $\Phi_{0} = 0.9$

$$\Rightarrow k' = 74.5 \, \mu A/V^2$$
PMOS:
\[ C_{ox} = 6 \, \text{fF/\mu m}^2 \]
\[ C_{o} = 0.27 \, \text{fF/\mu m} \]
\[ C_j = 1.9 \, \text{fF/\mu m}^2 \]
\[ m_j = 0.48 \]
\[ C_{jsw} = 0.22 \, \text{fF/m} \]
\[ m_{jsw} = 0.32 \]
\[ \Phi_0 = 0.9 \]

(2) Suppose in a FO4 inverter chain shown in Fig 2, the first stage and the second stage are connected by a 50\,\mu m long, 0.25\,\mu m wide poly wire (a huge mistake!). Use the equivalent capacitances you found in part (1) to calculate propagation delay \( T_{dLH} \) and \( T_{dHL} \). Assume \( R_w = 150 \, \Omega/\square \), \( C_w = 0.09 \, \text{fF/\mu m}^2 \), \( R_{eqN\text{MOS}} = 10 \, \text{k}\Omega \) and \( R_{eqP\text{MOS}} = 12 \, \text{k}\Omega \) for a unit size inverter. (10 pts)

Solution:

(1) \[ C_{g\text{inv}} = C_{g}\nu + C_{g\text{p}} = W_n L_n C_{ox} + W_p L_p C_{as} + 2 W_n C_o + 2 W_p C_o = 1.86 \, \text{fF} \]
\[ C_{g\text{invLH}} = C_{g\text{inv}} = 1.86 \, \text{fF} \]

For the junction capacitance, let’s first calculate \( K_{eq} \) using the following equation:
\[ K_{eq} = \frac{-\Phi_0^m}{(V_{high} - V_{low})(1 - m)}[(\Phi_0^m - V_{high})^{1-m} - (\Phi_0^m - V_{low})^{1-m}] \rightarrow \]
\[ K_{eqLH} = \frac{-0.9^{0.48}}{(2.5 + 1.25)(1 - 0.5)}[(0.9^{0.48} + 2.5)^{1-0.48} - (0.9^{0.48} + 1.25)^{1-0.48}] = 0.57 \]
\[ K_{eqLH} = \frac{-0.9^{0.48}}{(1.25 + 0)(1 - 0.5)}[(0.9^{0.48} + 1.25)^{1-0.48} - (0.9^{0.48} + 0)^{1-0.48}] = 0.77 \]
\[ K_{eqLH} = \frac{-0.9^{0.48}}{(2.5 + 1.25)(1 - 0.48)}[(0.9^{0.48} + 2.5)^{1-0.48} - (0.9^{0.48} + 1.25)^{1-0.48}] = 0.58 \]
\[ K_{eqLH} = \frac{-0.9^{0.48}}{(1.25 + 0)(1 - 0.48)}[(0.9^{0.48} + 1.25)^{1-0.48} - (0.9^{0.48} + 0)^{1-0.48}] = 0.78 \]
\[ K_{eqLH} = \frac{-0.9^{0.44}}{(2.5 + 1.25)(1 - 0.44)}[(0.9^{0.44} + 2.5)^{1-0.44} - (0.9^{0.44} + 1.25)^{1-0.44}] = 0.61 \]
\[ K_{eqLH} = \frac{-0.9^{0.44}}{(1.25 + 0)(1 - 0.44)}[(0.9^{0.44} + 1.25)^{1-0.44} - (0.9^{0.44} + 0)^{1-0.44}] = 0.79 \]
\[ K_{eqLH} = \frac{-0.9^{0.32}}{(2.5 + 1.25)(1 - 0.32)}[(0.9^{0.32} + 2.5)^{1-0.32} - (0.9^{0.32} + 1.25)^{1-0.32}] = 0.69 \]
\[ K_{eqLH} = \frac{-0.9^{0.32}}{(1.25 + 0)(1 - 0.32)}[(0.9^{0.32} + 1.25)^{1-0.32} - (0.9^{0.32} + 0)^{1-0.32}] = 0.84 \]

We can therefore calculate junction capacitances:
3. The following circuit in your midterm problem realizes a logic inverter. Because the “volristor” is still a highly-protected national secret, we are forced to use our old MOS transistor to realize the inverter.

![Figure 3 An inverter.](image)

(1) Do you choose NMOS or PMOS transistor to replace the “volristor” to realize the inverter? Briefly explain how your new inverter operates with a MOS transistor. (5 pts)

(2) Find $V_{OH}$, $V_{OL}$, and $V_M$ for the inverter you designed in (1). Assume $VDD=2.5V$, $R=100K\Omega$, and the transistor size $W/L=0.5\mu m/0.25\mu m$. Use the following model parameters from the textbook. (15 pts)

NMOS: $V_{TO}=0.43V$, $k_p'=115uA/V^2$, $\gamma=0.4V^{1/2}$, $\lambda=0.06V^{-1}$, $V_{DSAT} = 0.63V$
PMOS: \( V_T = -0.4 \, \text{V}, \ k_p' = 30 \, \text{uA/V}^2, \ \gamma = -0.4 \, \text{V}^{1/2}, \ \lambda = -0.1 \, \text{V}, \ V_{DSAT} = -1 \, \text{V} \)

(3) What is the sizing constraint of the transistor if we want \( V_{OH} \) higher than 2.4V? (5 pts)

**Solution:**

(1) Use PMOS transistor to replace the “volristor” to realize an inverter. When input goes high, the PMOS transistor is turned off and the output is pulled to ground via the resistor. When input goes low, the PMOS is turned on and the output is charged up toward VDD.

(2) Because the PMOS transistor can be completely turned off when \( V_{in} \) is larger than \( V_{DD} - V_T \).

\[ \Rightarrow V_{OL} = 0 \]

To calculate \( V_{OH} \), first assume that the PMOS transistor operates in the linear region when \( V_{in} = 0 \, \text{V} \) and \( V_{out} = V_{OH} \). We can solve the following equation:

\[ \frac{V_{OH}}{R} = k' \frac{W}{L} \left[ (V_{DD} - V_T)(V_{DD} - V_{OH}) - \frac{(V_{DD} - V_{OH})^2}{2} \right] \]

where \( R = 100 \, \text{K}\Omega \), \( k' = 30 \, \mu \Omega \), \( \frac{W}{L} = 2 \), \( V_{DD} = 2.5 \), \( V_T = 0.4 \)

\[ \Rightarrow V_{OH} = 2.31 \, \text{V} \]

We can double check that the PMOS indeed operates in the linear region and our assumption is valid.

Final check: \( V_{OH} = f(V_{OL}) \) and \( V_{OL} = f(V_{OH}) \), which means our calculation is correct.

For the calculation of \( V_M \), first assume that the PMOS transistor operates in the saturation region when \( V_{in} = V_{out} = V_{M} \). We can then solve the following equation:

\[ \frac{V_M}{R} = \frac{1}{2} k' \frac{W}{L} (V_{DD} - V_M - V_T)^2 \]

\[ \Rightarrow V_M = 1.41 \, \text{V} \]

Again, we double check that the PMOS operates in the saturation region and our assumption is valid.

(3) When \( V_{in} = 0 \, \text{V} \) and \( V_{out} > 2 \, \text{V} \), the PMOS transistor operates in the linear region. We can solve the following two equations:

\[ \frac{V_{OH}}{R} = k' \frac{W}{L} \left[ (V_{DD} - V_T)(V_{DD} - V_{OH}) - \frac{(V_{DD} - V_{OH})^2}{2} \right] \]

\[ V_{OH} > 2.4 \, \text{V} \]

where \( R = 100 \, \text{K}\Omega \), \( k' = 30 \, \mu \Omega \), \( \frac{W}{L} = 2 \), \( V_{DD} = 2.5 \), \( V_T = 0.4 \)

\[ \Rightarrow \frac{W}{L} > 3.9 \]