Introduction

In Phase 2 of the project, we will design the row decoder for the 4Mb SRAM array introduced in Phase 1. System block diagram is shown below in Fig. 1. A row decoder decodes the 10-bit address input and enables access to one of the 1,024 rows at a time. Objective of Phase 2 is to minimize decoder energy consumption while meeting layout and performance requirements.

Fig. 1 A 4Mb SRAM Array with Error Correction.

Layout Constraints

An SRAM cell is made of 6 transistors (schematic and layout in Fig. 2 and Fig. 3 respectively), downloadable from ~ee141/sp09/project/sram/. Height of the cell is 2.49 um (note that half of the VDD and bit line contacts are shared with adjacent rows above and below).
Fig. 2 Schematic of the 6-Transistor SRAM Cell.

Fig. 3 Layout of the SRAM Cell.
Given the large number of input bits, it is advisable to split the row decoder to two parts: pre-decoder and final decoder. You are asked to perform following specific tasks:

1. Download the SRAM cell layout from the class project directory (~ee141/sp09/project/sram/cell) and follow the tutorial on the project website (http://bwrc.eecs.berkeley.edu/Classes/ICDesign/EE141_s09/Project/ParasiticExtraction.htm) to extract MOS and R-C models from the layout.

2. When configuring simulation schematics, instantiate the SRAM cell using its layout extracted model and name the instance to include total number of identical cells in a row (don’t forget the parity bits from Phase 1). This will represent overall loading to the row decoder.

3. Design the schematic of the row decoder to meet the delay and layout requirements. Minimize the decoder’s power consumption. Details about delay and power consumption will be specified in next sections.

4. Design the layout of the final decoder. Demonstrate that the final decoder’s pitch matches the SRAM’s height. The final decoder + SRAM cell layout must pass LVS.

5. Design the floor plan of the pre- and final decoders and the wiring in between. While you don’t need to draw layout for the pre-decoder or the wires, you will need to estimate the wire capacitance for delay and power simulation using the process data given in Tables 1 and 2. We will ignore wire resistance in this case.

<table>
<thead>
<tr>
<th></th>
<th>Field</th>
<th>Poly</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Poly</strong></td>
<td>Area (aF/um²)</td>
<td>105</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fringe (aF/um)</td>
<td>45</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>M1</strong></td>
<td>Area (aF/um²)</td>
<td>49</td>
<td>115</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fringe (aF/um)</td>
<td>36</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>M2</strong></td>
<td>Area (aF/um²)</td>
<td>28</td>
<td>32</td>
<td>86</td>
<td></td>
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<tr>
<td></td>
<td>Fringe (aF/um)</td>
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<td>5.0</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td><strong>M3</strong></td>
<td>Area (aF/um²)</td>
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<td>17</td>
<td>27</td>
<td>86</td>
</tr>
<tr>
<td></td>
<td>Fringe (aF/um)</td>
<td>26</td>
<td>2.8</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td><strong>M4</strong></td>
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<td>12</td>
<td>16</td>
<td>28</td>
</tr>
<tr>
<td></td>
<td>Fringe (aF/um)</td>
<td>24</td>
<td>1.9</td>
<td>4.5</td>
<td>8.4</td>
</tr>
</tbody>
</table>

Table 1. Layer-to-Layer Wire Capacitance.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Poly</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capcitance (aF/um)</td>
<td>100</td>
<td>99</td>
<td>101</td>
<td>102</td>
<td>77</td>
</tr>
</tbody>
</table>

Table 2. Same-Layer Wire Capacitance (Minimum Spacing).
Propagation Delay

Unlike in Phase 1, you are now encouraged to use any logic style or a combination of multiple styles in Phase 2. You can also use as many clocks as you like for this design. Specifications on the clocks include:

- Clock frequency: 100MHz;
- Duty cycle: 50%;
- Rise and fall time: 50ps.

Note that you will need at least one clock for this design, which is the enable signal (EN, active high) to pre-charge the bit lines after a successful read or write operation. Assume that the EN signal goes high at the same time when the input address bits make transition.

You are also given the freedom to choose the supply voltage:

- $V_{DD}$: 0.7 ~ 1V

The lower bound is to ensure sufficient signal to noise ratio; the upper bound is to prevent device breakdown.

Simulation schematic for propagation delay and power consumption needs to be constructed in a hybrid fashion:

- Identify the critical path for propagation delay and an input pattern that excites it;
- Use layout extracted SRAM model as external loading (see previous section). Connect all bit lines to $V_{DD}$;
- Estimate the wiring capacitance from Tables 1 and 2 and model those as lumped capacitors;
- Add external and internal (wiring) loading to the decoder schematic for simulation.

Again you don’t need to construct the entire decoder for this project. Instead it is only the schematic of the critical path that is required. When there are multiple fan-in and fan-out gates however, you need to include 2 stages of off-path in the simulation schematic to characterize propagation delay more accurately.

Input capacitance of the row decoder should not exceed $4C$, where $C$ is the input capacitance of a unit-size inverter (NMOS: 120n/100n, PMOS: 240n/100n).

Propagation delay of the critical path should not exceed 2ns.

Power Consumption

Schematic for power consumption simulation is identical to that for propagation delay simulation. Estimate the total decoder power by scaling from the simulation result. Also be reminded that when clocks are used their loading capacitance and power consumption need to be included in the overall power budget too.
Report

Please use the report template provided at the website. Be sure to justify important design decisions and emphasize all the vital information. Organization, conciseness, and completeness are of paramount importance. Good reports are short and to the point. Make sure to include and annotate important plots to illustrate your effort. Do not repeat the information we already know. Make sure to fill out the cover-page and use the correct units.

Grading

Quality of reporting is a major part of the grade. For Phase 2, the grade will be equally divided over the correctness and completeness of the results, and quality of the report.

Have fun, and good luck!