[PROBLEM 1] Logic Styles and Logical Effort (30 pts)
In this problem, you can assume that $C_D = C_O = 2fF/\mu$m, and $R_{eq\text{NMOS}} = 10k\Omega$, $R_{eq\text{PMOS}} = 20k\Omega$, for the minimum-size NMOS and PMOS transistors (size=1).
(a) What logical function does the gate shown below perform? (5 pts)

(b) Given the sizing show below, what value of $W$ would you use in order to make the worst-case LE of the C input equal to half of the LE of A and B inputs (i.e., $LE_C = 1/2 \ LE_A$) What would be the LE of the C input in this case? (5 pts)

(c) Use ratioed logic to implement the same logic function in (a). Size the transistors such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio is 2/1). The size of load PMOS is 1. What is the LE of input A, B and C? (10 pts)

(d) Use dynamic logic to implement the same logic function in (a). Size the transistors such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio is 2/1). The size of the evaluation NMOS transistor (connected to clock in pull-down network) is the same as the size of other NMOS transistors in PDN. What is the LE of input A, B and C during evaluation phase? (10 pts)
[PROBLEM 2] Dynamic Logic Design (45 pts)

In this problem, you can assume that VDD = 1.2 V, $C_D = C_G = 2fF/\mu m$, and $V_T = 0.2 V$.

(a) In the domino gate shown below, what is the minimum $W_n$ necessary to ensure that the gate does not fail due to charge sharing? You can assume that the $V_{IH}$ of the inverter is $\frac{3}{4} VDD$, and none of the source/drain regions have been shared (10 pts)

(b) In order to mitigate the charge sharing issue, what can we change in the gate from (a)? You should explain your changes and draw new transistor-level schematics of the gate (no sizing necessary). (15 pts)

(c) On the evaluation phase, what is the delay of the dynamic gate as a function of $R_{eqNMOS}$, $R_{eqPMOS}$, $C_G$ and $C_L$? $R_{eqNMOS}$ and $R_{eqPMOS}$ are the equivalent resistances of minimum size NMOS and PMOS. You can assume $C_D = 0$ and ignore the slope effect. (10 pts)

(d) What are the activity factor of node Out if $P(A=0) = P(B=0) = P(C=0) = 0.25$? (Bonus 5 pts)

(e) Charge leakage at node Out may cause problems. What is the solution to resolve this issue? (5 pts)
[PROBLEM 3] Timing (30pts)
In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figures, and the registers have the following properties: $t_{\text{clk-q}} = 50\text{ps}$, $t_{\text{setup}} = 25\text{ps}$, and $t_{\text{hold}} = 40\text{ps}$. You can assume that the clock has no jitter.

(a) What is the minimum clock cycle time of this pipeline? Are there any hold time violations? (10pts)

(b) Now we insert the repeaters for distributing the clock signal to three registers. Assume that the delay of each repeater is nominally 50ps and each repeater’s delay varies randomly by +/- 20%, now what is the minimum clock cycle time of this pipeline? Are there any hold time violations? (10 pts)

(c) Under the same conditions (i.e., 50ps nominal inverter delay and +/-20% delay variation), if we feed the clock from the other direction, what is the minimum clock cycle time of this pipeline? Are there any hold time violations? (10 pts)