You should write your results on the exam sheets only. Partial credit will be given only if you show your work and reasoning clearly.

Throughout the exam, you can ignore the $r_o$ of any transistors and all capacitors except those explicitly drawn in the diagrams unless the problem states otherwise.

Name: __________________________________________

SID: __________________________________________
Problem 1 (24 points) Offset and Noise

a) (3 pts) Due only to the mismatch between M1 and M2, what is the variance of the input-referred voltage offset of the amplifier shown below? You can assume that M1/M2 and M3/M4 are nominally perfectly matched – i.e., \( V_{M1^*} = V_{M2^*} = V_{N^*}, \)
\( V_{M4^*} = V_{M4^*} = V_{P^*} \). You should provide your answer in terms of \( V_{N^*}, V_{P^*}, \) \( A_{Vth}, A_{f}, \) and \( W_N, L_N, W_P, \) and \( L_P \) (i.e., the dimensions of the devices).

![Amplifier Diagram](image)

b) (5 pts) Now due only to the mismatch between M3 and M4, what is the variance of the input-referred voltage offset of the same amplifier (repeated below)?
c) **(4 pts)** What is the variance of the thermal noise at the output of the amplifier when it is driving a capacitive load (shown below)? You can assume that the current source is ideal (i.e., noiseless). You should provide your answer in terms
of $kT$, $C_L$, $V_{N^*}$, $V_{P^*}$, and $\gamma$. (Hint: If you broke the negative feedback, what would be the $nf$ of the amplifier?)

d) **(8 pts)** Due only to the noise current from M1, what is the variance of the thermal noise at $V_{out}$ after including the capacitance of the PMOS load devices ($C_M$)?
e) **(4 pts)** Now let’s replace the ideal current source with a real transistor (M5 below). At DC, what percentage of the thermal noise current from M5 leads to voltage noise at $V_{out}$? If $g_{mM3}/C_M << g_{mM2}/C_L$, what percentage of the noise current from M5 leads to voltage noise at $V_{out}$ at high frequencies (relative to $g_{mM3}/C_M$)?
Problem 2 (18 points) Settling Time and Data Rate

This problem will examine the conceptual link shown below, where the channel is modeled by the R1/C1 network. Throughout this problem, you can assume that the channel itself is noiseless, that the receiver has infinite bandwidth, and that the transmitter has a peak-to-peak voltage swing of 2V_{sw} (i.e., the TX output ranges from –V_{sw} to +V_{sw}).

\[ \tau_1 = R_1 C_1 \]

a) **(4 pts)** If the receiver does not use any equalization but is otherwise perfect (i.e., does not have any input-referred offset or noise), what is the minimum bit-period T_{bit} you can achieve with this link without making any errors (i.e., BER=0)? You should provide your answer in terms of \( \tau_1 = R_1 C_1 \).
b) \textbf{(6 pts)} Still assuming no equalization, what is the minimum $T_{\text{bit}}$ if the receiver needs to achieve a BER of $10^{-12}$ with an input referred offset equal to $V_{\text{off}}$ and input-referred noise standard deviation ($\sigma$) of $\sigma_{n_{\text{rx}}}$? You should provide your answer in terms of $V_{\text{sw}}$, $\tau_1$, $V_{\text{off}}$, and $\sigma_{n_{\text{rx}}}$. 
c) (8 pts) One crude (and usually impractical) way of implementing “equalization” is to add a capacitor $C_2$ as shown below. For the same BER, offset, and noise as part b), what is the minimum $T_{\text{bit}}$ with this capacitor included? You should provide your answer in terms of $V_{sw}$, $\tau_1$, $V_{off}$, $\sigma_{n_{rx}}$, and $k_c = C_2/C_1$.

![Diagram of equalization circuit with capacitors $C_1$, $C_2$, $R_1$, and TX and RX symbols]
Problem 3 (14 points) Latch Design

In this problem we will be looking at the CML latch shown below. All of the devices have minimum channel length; the widths of M1, M2, M3, and M4 are chosen to achieve a fixed $V^*$ of 200mV. You can assume that M5 and M6 operate as ideal switches.

Unless otherwise noted, you should use the following design and technology parameters:

- $R_L = 1k\Omega$
- $I_b = 400\mu A$
- For $V^* = 200mV$, $I_{DS/W} = 20\mu A/\mu m$.
- $C_{gg} = 2fF/\mu m$ of width
- $C_{dd} = 1fF/\mu m$ of width.
- $V_{DD} = 1.2V$

a) **(3 pts)** Ignoring all capacitive loading except from the latch devices themselves, what is the bandwidth of the latch while M5 is on and M6 is off?
b) **(1 pts)** What is the peak-to-peak differential voltage swing at the output of the latch when M5 is off and M6 is on?

c) **(6 pts)** When M5 turns on, the latch not only starts to amplify the new input, it also begins resetting the previously latched voltage back to zero. Assuming that the output of the latch was previously a 1, write an expression for the differential output of the latch $V_{o,\text{diff}}$ as a function of the differential input voltage $V_{i,\text{diff}}$ (which you can assume is a step) and the length of time that M5 is turned on ($t_{M5}$).
d) **(4 pts)** Given your answers to the previous sections, what is the input-referred hysteresis of the latch if $t_{s5} = 200$ ps?
Problem 4 (12 points) Miscellaneous

a) (6 pts) One of your colleagues suggests biasing an amplifier using the configuration shown below. Is this bias loop stable? If so, you should predict the bias point of the design. If not, explain the source of the instability.

![Amplifier Circuit Diagram]
b) (6 pts) If the NMOS sampling switch with the input and gate voltage swings shown below must achieve a worst-case sampling time constant of $\tau_{\text{req}}$, what is the worst-case voltage error at $V_o$ due to charge injection? You can assume a quadratic transistor model with $I_D = \mu C_{\text{ox}} (W/L)(V_{\text{gs}} - V_{\text{th}} - V_{\text{ds}}/2) \cdot V_{\text{ds}}$. You should provide your answer in terms of the device parameters, $V_{\text{dd}}$, $V_{\text{sw}}$, $C_L$, and $\tau_{\text{req}}$. 

![Diagram of NMOS sampling switch with voltage swings](image-url)