You should write your results on the exam sheets only. Partial credit will be given only if you show your work and reasoning clearly.

Name: ____________________________

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Problem 1 (13 points) Capacitance and SNR

In this problem we will look at optimizing the SNR of the amplifier shown below.

You should use the following assumptions and simplifications to solve this problem:

- The input of the amplifier ($V_{in}$) is a sinusoid with an angular frequency of $\omega_{in}$ and an amplitude of $A_{in}$.
- The transistor is biased with a fixed $V*$ so that its gain ($g_{m}r_{0}$) is $A_{v0}$.
- Assume $R_s$ is noiseless, and ignore all capacitors except those shown in the figure.
- You should assume that $1/(r_{o}C_{d}) \gg \omega_{in}$. In other words, $V_{out}(j\omega_{in})/V_{g}(j\omega_{in}) = A_{v0}$.
- Your final answers should be a function of only $k$, $T$, $\gamma$, $\omega_{in}$, $A_{in}$, $k_{d}$, $A_{v0}$, $R_{s}$, and $C_{gs}$.

a) (4 pts) What is the voltage noise variance $\overline{v_{in}^2}$ at the output of the amplifier?

No noise from $R_{s}$, so just look at output node:

\[ \overline{v_{in}^2} = \frac{kT}{C_{d}} \cdot \frac{1}{4r_{o}C_{d}} \]
\[ \overline{v_{o}^2} = \frac{kT}{C_{d}} \cdot 8A_{v0} \]
\[ \overline{v_{og}^2} = \frac{kT}{C_{gs}} \cdot \frac{8A_{v0}}{k_{d}} \]
b) **(4 pts)** What is the mean-squared signal voltage $\overline{V_{out}^2}$ at the output of the amplifier?

\[
\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1 - sR_sC_{gs}}
\]

\[
\left| \frac{V_g(j\omega)}{V_{in}(j\omega)} \right|^2 = \frac{1}{1 + \omega^2 R_s^2 C_{gs}^2}
\]

\[
V_{out} = A_v V_g \quad \overline{V_{in}^2} = \frac{A_v^2}{2}
\]

\[
\overline{V_{out}^2} = A_{v0}^2 \cdot \frac{A_v^2}{2} \cdot \frac{1}{1 + \omega^2 R_s^2 C_{gs}^2}
\]
c) (5 pts) Keeping the $V^*$ of the transistor fixed, what value of $C_{gs}$ maximizes the $\text{SNR} \frac{\overline{V_{out}^2}}{\overline{V_{in}^2}}$ at the output of the amplifier?

\[
\frac{\overline{V_{out}^2}}{\overline{V_{in}^2}} = \frac{A_{vu}^2 \cdot A_w}{(1 - W_{in}^2 R_s^2 C_{gs}^2)} \cdot \frac{C_{gs}}{kT} \cdot \frac{k_d}{8 A_{vu}}
\]

\[
\text{SNR} \propto \frac{C_{gs}}{1 - W_{in}^2 R_s^2 C_{gs}^2} \quad (A_{vu} \text{ does not change with } C_{gs} \text{ since } V^* \text{ is fixed})
\]

\[
\frac{\partial \text{SNR}}{\partial C_{gs}} = \frac{(1 - W_{in}^2 R_s^2 C_{gs}^2) - 2 C_{gs} W_{in}^2 R_s^2 C_{gs}^2}{(1 - W_{in}^2 R_s^2 C_{gs}^2)^2} = 0
\]

\[
1 + W_{in}^2 R_s^2 C_{gs}^2 = 2 W_{in}^2 R_s^2 C_{gs}^2
\]

\[
W_{in} R_s^2 C_{gs}^2 = 1
\]

\[
C_{gs} = \frac{1}{W_{in} R_s}
\]

(i.e., $W_{in} = \frac{1}{R_s C_{gs, opt}}$)
Problem 2 (10 points) Noise

Considering only the noise current from M₃, what is the variance of the differential voltage noise at the output of the amplifier shown below? You can ignore all the rₜ's of the transistors and all capacitors except those explicitly drawn in the schematic. You can assume that M₁ and M₂ are identical (i.e., \( g_{m1} = g_{m2} \)), and you should provide your answers in terms of \( k, T, \gamma, C_L, (g_{m3}/g_{m1}), (\Delta R/R), \) and \( A_{v,nom} = (g_{m1}R) \).

\[ V_{o+} = \frac{I_{n3}}{2} \cdot \frac{R+\Delta R}{1+s(R+\Delta R)C_L} \]
\[ V_{o-} = \frac{I_{n3}}{2} \cdot \frac{R}{1+sRC_L} \]
\[ V_{o,diff} = V_{o+} - V_{o-} = \frac{I_{n3}}{2} \cdot \frac{(R+\Delta R)(1+sRC_L) - R(1+s(R+\Delta R)C_L)}{(1+s(R+\Delta R)C_L)(1+sRC_L)} \]

\[ \frac{V_{o,diff}}{I_{n3}} = \frac{\Delta R/2}{s^2 R(R+\Delta R)C_L^2 + sRC_L(2+\frac{\Delta R}{R}) + 1} \]

\[ \frac{V_{o,diff}}{I_{n3}} = \frac{4kT \gamma g_{m3} \cdot \frac{\Delta R^2}{4} \cdot \frac{1}{4RCL(2+\frac{\Delta R}{R})}}{\gamma g_{m3} \cdot \frac{\Delta R}{2+\frac{\Delta R}{R}}} \]

So:

\[ V_{o,diff} = \frac{kT \gamma A_{v,nom} \cdot \left( g_{m3}/g_{m1} \right) \cdot \frac{(\Delta R/R)^2}{(2+\Delta R/R)}}{4C_L} \]
Problem 3 (9 points) Amplifier Design

\[ i_{n_{in},tot}^2 = i_{n_{in},m1}^2 \cdot M^2 + i_{n_{in},m2}^2 \cdot M^2 + i_{n_{in},m3}^2 \]

\[ \eta_f = \frac{i_{n_{in},tot}^2}{i_{n_{in},m1}^2 \cdot M^2} = 1 + \frac{i_{n_{in},m2}^2}{i_{n_{in},m1}^2} + \frac{i_{n_{in},m3}^2}{i_{n_{in},m1}^2 \cdot M^2} \]

\[ i_{n_{in},m1}^2 = 4kT \delta g_{m1} \Delta \theta \]
\[ i_{n_{in},m2}^2 = 4kT \delta g_{m2} \Delta \theta \]
\[ i_{n_{in},m3}^2 = 4kT \delta g_{m3} \Delta \theta \]

\[ S_0 = \eta_f \left( 1 + \frac{g_{m2}}{g_{m1}} + \frac{Mg_{m2}}{M^2 g_{m1}} \right) \]

\[ \eta_f = 1 + \left( 1 + \frac{1}{M} \right) \cdot \frac{V_n^*}{V_p^*} \]
b) (5 pts) Now let’s look at the stability of this amplifier under feedback using the model shown above (ignore the $r_0$’s and all capacitors except the ones shown in the model). If the amplifier is placed into unity-gain feedback with a closed-loop bandwidth of $\omega_{gbw}$, what is the maximum $M$ that will provide at least 45° of phase margin? You should provide your answer in terms of $\omega_{gbw}$ and the $\omega_T$ of the PMOS transistors.

Pole at $V_{mirror}$: $\omega_{p2} = \frac{g_{m2}}{(1-M)C_{gs2}} = \frac{\omega_T}{(1+M)}$

$\omega_{p2}$ is the non-dominant pole.

Dominant pole crosses over at $\omega_{gbw}$ ($= \frac{g_{m1}}{C_L}$)

For $\geq 45^\circ$ phase margin want:

$\omega_{p2} \geq \omega_{gbw}$

$$\frac{\omega_T}{1-M} \geq \omega_{gbw}$$

$M \leq \frac{\omega_T}{\omega_{gbw}} - 1$