Today’s Lecture

- EE240 CMOS Technology

- Passive devices
  - Motivation
  - Resistors
  - Capacitors
  - (Inductors)

- Next time: MOS transistor modeling
EE240 Process

- 90nm 1P7M CMOS
  - Minimum channel length: 90nm
  - 1 level of polysilicon
  - 7 levels of metal (Cu)
  - 1.2V supply
  - Models for this process not “real”

- Other processes you might see
  - Shorter channel length (45nm / 1V)
  - Bipolar, SiGe HBT
  - SOI

Process Options

- Available for many processes

- Add features to “baseline process”

- E.g.
  - Silicide block option
  - “High voltage” devices (2.5V & 3.3V, >10V)
  - Low $V_{TH}$ devices
  - Capacitor option (2 level poly, MIM)
  - ...

CMOS Cross Section

- Metal
- p⁻ substrate
- p⁺ diffusion
- Poly
- n⁻ well
- n⁺ diffusion

Dimensions

- 1.4 nm
- ≥ 90 nm
- 50 nm
- 0.6 μm
- 700 μm
Why Talk About Passives?

Resistors

- No provisions in standard CMOS
- Resistors are bad for digital circuits →
  - Minimized in standard CMOS
  - But, often want big, well-controlled R for analog…
- Sheet resistance of available layers:

<table>
<thead>
<tr>
<th>Layer</th>
<th>Sheet resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>60 mΩ/□</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>5 Ω/□</td>
</tr>
<tr>
<td>N+/P+ diffusion</td>
<td>5 Ω/□</td>
</tr>
<tr>
<td>N-well</td>
<td>1 kΩ/□</td>
</tr>
</tbody>
</table>
How about an N-Well Resistor?

Silicide Block Option

<table>
<thead>
<tr>
<th>Layer</th>
<th>$\frac{R}{\square} [\Omega/\square]$</th>
<th>$T_C [\text{ppm/}^\circ\text{C}]$ @ $T = 25$ $^\circ\text{C}$</th>
<th>$V_C [\text{ppm/V}]$</th>
<th>$B_C [\text{ppm/V}]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N+ poly</td>
<td>100</td>
<td>800</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>P+ poly</td>
<td>180</td>
<td>200</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>N+ diffusion</td>
<td>50</td>
<td>1500</td>
<td>500</td>
<td>-500</td>
</tr>
<tr>
<td>P+ diffusion</td>
<td>100</td>
<td>1600</td>
<td>500</td>
<td>-500</td>
</tr>
<tr>
<td>N-well</td>
<td>1000</td>
<td>-1500</td>
<td>20,000</td>
<td>30,000</td>
</tr>
</tbody>
</table>

- Non-silicided layers have significantly larger sheet resistance
- Even with silicide block, many non-idealities:
  - Temperature coefficient: $R = f(T)$
  - Voltage coefficient: $R = f(V)$
  - Manufacturing Variations
Resistor Temp-Co. Example

Voltage Dependence
**Voltage Coefficient**

Example:

**Diffusion resistor**

→ **Applied voltage modulates depletion width**
   (cross-section of conductive channel)

→ **Well acts as a shield**

\[
R \approx \frac{V_1 - V_2}{I} \\
= R_0 \left[ 1 + T_c \left( T - 25^\circ \right) + V_c (V_1 - V_2) + B_c \left( \frac{V_1 + V_2}{2} - V_a \right) \right]
\]

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**Compensation**
Resistor Matching

- Types of mismatch:
  - Run-to-run variations
    - Global differences in thickness, doping, etc.
  - Systematic (e.g. contacts)
  - Random variations between devices

- Run-to-run variations in absolute R value: 20+% 
  - Can be problematic for termination, bias current, etc.

- Best case: make circuit depend only on ratios
  - E.g., use feedback to control opamp gain
  - With careful layout, can get 0.1 – 1% matching

Systematic Variations from Layout

- Example:

\[
\begin{align*}
R & \quad \text{R} \\
2R? & \quad \text{2R?} \\
2R & \quad \text{2R} \\
R & \quad \text{R}
\end{align*}
\]

- Use unit element instead:
Common Centroid and Dummies

Example: \( R_1 : R_2 = 1 : 2 \)

\[
\begin{align*}
\text{Dummy} \rightarrow & \quad 0.5 \times R_2 - \Delta R \\
\text{Dummy} \rightarrow & \quad 0.5 \times R_2 + \Delta R \\
\text{Dummy} \rightarrow & \quad 0.5 \times R_2 - \Delta R
\end{align*}
\]

Resistor Layout (cont.)

Serpentine layout for large values:

Better layout (mitigates offset due to thermoelectric effects):

MOSFETs as Resistors

- **Triode region ("square law"):**
  \[ I_d = \mu C_{ov} \frac{W}{L} \left( V_{gs} - V_{th} - \frac{V_{ds}}{2} \right) \]
  for \( V_{gs} - V_{th} > V_{ds} \)

- **Small signal resistance:**
  \[ \frac{1}{R} = \frac{\partial I_d}{\partial V_{ds}} = \mu C_{ov} \frac{W}{L} (V_{gs} - V_{th} - V_{in}) \]
  \[ R \approx \frac{1}{\mu C_{ov} \frac{W}{L} (V_{gs} - V_{th})} \quad \text{for} \quad V_{gs} - V_{th} >> V_{ds} \]

- **Voltage coefficient:**
  \[ V_c = \frac{1}{R} \frac{\partial R}{\partial V_{ds}} = \frac{1}{V_{gs} - V_{th} - V_{ds}} \]

MOS Resistors

**Example:** \( R = 1 \text{ M}\Omega \)

\[ R = \frac{1}{\mu C_{ov} \frac{W}{L} (V_{gs} - V_{th})} \]
\[ W = \frac{1}{\mu C_{ov} R (V_{gs} - V_{th})} = \frac{1}{100 \mu A \times 1 \text{M}\Omega \times 2 \text{V}} = \frac{1}{200} \]
\[ V_c \bigg|_{V_{in} = 0} = \frac{1}{V_{gs} - V_{th}} = \frac{1}{2 \text{V}} \approx 0.5 \text{V}^{-1} \]

- **Large R-values realizable in small area**
- **Very large voltage coefficient**

**Applications:**
- **MOSFET-C filters: (linearization)**

- **Biasing:** (>1G\Omega)
Resistor Summary

• No or limited support in standard CMOS
  • Large area (compared to FETs)
  • Nonidealities:
    • Large run-to-run variations
    • Temperature coefficient
    • Voltage coefficients (nonlinear)

• Avoid them when you can
  • Especially in critical areas, e.g.
    • Amplifier feedback networks
    • Electronic filters
    • A/D converters
  • We will get back to this point

Capacitors

• Simplest capacitor:

  substrate

• What’s the problem with this?
Capacitors

- “Improved” capacitor:

- Is this only 1 capacitor?

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Capacitor Options

<table>
<thead>
<tr>
<th>Type</th>
<th>C [aF/µm²]</th>
<th>$V_C$ [ppm/V]</th>
<th>$T_C$ [ppm/°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate</td>
<td>10,000</td>
<td>Huge</td>
<td>Big</td>
</tr>
<tr>
<td>Poly-poly</td>
<td>1000</td>
<td>10</td>
<td>25</td>
</tr>
<tr>
<td>(option)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal-metal</td>
<td>50</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>Metal-substrate</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal-poly</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Poly-substrate</td>
<td>120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction caps</td>
<td>~ 1000</td>
<td>Big</td>
<td>Big</td>
</tr>
</tbody>
</table>
MOS Capacitor

- High non-linearity, temperature coefficient
- But, still useful in many applications, e.g.:
  - (Miller) compensation capacitor
  - Bypass capacitor (supply, bias)

Capacitor Layout

- Unit elements
- Shields:
  - Etching
  - Fringing fields
- “Common-centroid”
- Wiring and interconnect parasitics

MIM Capacitors

- Some processes have MIM cap as add-on option
  - Separation between metals is much thinner
  - Higher density

- Used to be fairly popular
  - But not as popular now that have many metal layers anyways

Capacitor Geometries

- Horizontal parallel plate
- Vertical parallel plate
- Combinations

“MOM” Capacitors

- Metal-Oxide-Metal capacitor. Free with modern CMOS.
- Use lateral flux ($\sim L_{\text{min}}$) and multiple metal layers to realize high capacitance values

MOM Capacitor Cross Section

- Use a wall of metal and vias to realize high density
- More layers – higher density
  - May want to chop off lower layers to reduce $C_{\text{bot}}$
- Reasonably good matching and accuracy
Distributed Effects

- Can model IC resistors as distributed RC circuits.

- Could use transmission line analysis to find equivalent 2-port parameters.

- Inductance negligible for small IC structures up to ~10GHz.

\[ R \gg \omega L \]

Effective Resistance

- High frequency resistance depends on \( W \), e.g.:
  - \( W=1\mu \) 10k\( \Omega \) resistor works fine at 1GHz
  - \( W=5\mu \) 10k\( \Omega \) resistor drops to 5k\( \Omega \) at 1 GHz

- May need distributed model for accurate freq response
Capacitor Q

- Current density drops as you go farther from contact edge...

Double Contact Structure

- If contact on both edges,
  - $R$ drops 4X
  - Can be a good idea even if not hitting distributed effects
What About Inductors?

- Mostly not used in analog/mixed-signal design
  - Usually too big
  - More of a pain to model than R’s and C’s
  - But they do occasionally get used
- Example inductor app.: shunt peaking
  - Can boost bandwidth by up to 85%!
  - Q not that important (L in series with R)
  - But frequency response may not be flat

Spiral Inductors

- Used widely in RF circuits for small L (~1-10nH).
- Use top metal for Q and high self resonance frequencies.
  - Very good matching and accuracy – if you model them right