Offset

- To achieve zero offset, comparator devices must be perfectly matched to each other
- How well-matched can the devices be made?
  - Not arbitrary – direct function of design choices

Sources of Local Variation

- Deterministic sources:
  - Local poly density
  - Sub-90nm: stress, litho interactions, ...

- Random sources:
  - Dopant fluctuations
  - Line-edge roughness
  - Oxide traps

- Focus our modeling on random variations
  - Deterministic handled with good layout practices

Device Mismatch Categories

- Die-to-die
  - All devices on same chip (or wafer) have same characteristics

- Within die (long-range)
  - All devices within certain region have same characteristics

- Local (short-range)
  - Every device different, random
  - Usually most important source of mismatch

References

  - Mismatch model
  - Statistical data for 2.5µm CMOS

  - 0.18µm CMOS data

Mismatch Statistics

- Total mismatch set by composite of many single, independent events
  - Correlation distance << device dimensions
  - E.g., number of dopant atoms implanted into the channel

- Individual effects are small: linear superposition holds

- Mismatch is zero mean, Gaussian distribution
Parameter Mismatch Model

\[ \sigma^2(\Delta P) = \frac{A_s^2}{WL} + S_s^2 D_x^2 \]

- \(\sigma^2(\Delta P)\): variance of \(P\)
- \(WL\): active gate area
- \(D_x\): distance between device centers
- \(A_s\): measured area proportionality constant
- \(S_s\): measured distance proportionality constant,
  \[ \cong 0 \] for “good” layout

Back-Gate Bias, \(V_{SB}\)

- Mismatch can depend on \(V_{SB}\)
- Why?

\[ \sigma^2(\Delta V_T) = \frac{A_{T,MAX}}{WL} + S_{T}^2 \Delta V_T^2 \]

2.5\(\mu\)m CMOS process:

- \(A_{T,MAX} \approx 30 \text{ mV} / \mu\text{m}\)
- \(A_{T,MIN} \approx 35 \text{ mV} / \mu\text{m}\)

\(V_T\) Mismatch

- Mismatch in \(V_T\) between two identical devices:

\[ \sigma^2(\Delta V_T) = \frac{A_{T,MAX}^2}{WL} + S_{T}^2 \Delta V_T^2 \]

\(\Delta V_T\) largely independent of \(V_{DS}\)

\[ \beta = \mu C_{ox} \frac{W}{L} \]

\(\Delta V_T\) Mismatch

- Often largest source of offset

Current Matching, \(\Delta I_D/I_D\)

- Strong bias dependence (we knew that already)
Sources of $\beta$ Mismatch

- Mobility variations
  - E.g., due to dopant variations, random defects
- Oxide thickness variation
  - Usually very well-controlled
- Edge roughness

Edge Model

\[
\frac{\sigma^2(\beta)}{\beta^2} = \frac{\sigma^2(W)}{W^2} + \frac{\sigma^2(L)}{L^2} + \frac{\sigma^2(C_{ox})}{C_{ox}^2} + \frac{\sigma^2(\mu_s)}{\mu_s^2}
\]

For: \(\sigma^2(W) \propto \frac{1}{L}\) and \(\sigma^2(L) \propto \frac{1}{W}\)

Simplifies to:

\[
\frac{\sigma^2(\beta)}{\beta^2} \propto \frac{\mu_s^2}{W L} + \frac{\mu_s^2}{W L} + \frac{\mu_s^2}{W L} + S_J D^2\]

Distance Effect

Process Dependence

- $A_{ox}$ tends to scale with technology
- Proportional to $t_{ox}$
- Also depends on doping level

Orientation Effects

- Si and transistors are not (perfectly) isotropic
- \(\Rightarrow\) keep direction of current flow same!

0.18 $\mu$m CMOS
Current Matching

Voltage Matching

Common Centroid Layout

- Cancels linear gradients
- Required for moderate matching

Simulating Mismatch

- Brute force: Monte Carlo
- HSPICE “throws the dice”...

“Golden Rule” of Layout for Matching

- Everything you can think of might matter
  - Even whether or not there is metal above the devices
- How to avoid systematic errors?