Clock Generation

- Typical (low-cost) crystals give <500 MHz clock
  - 5 Gb/s link → where to get a 5 GHz clock?

- PLL: multiply frequency up, align phase
  - While maintaining low jitter, power
PLL: Linear Model

Ref_clk (from crystal) → PFD → Loop Filter → VCO → Clk

Fb_clk → +N

Linear Model cont’d
Stability and Loop Bandwidth

Loop Components: Phase Detectors

- Basic idea: create pulses with width $\alpha$ to phase difference
Loop Filter

VCOs
Noise and Jitter

• Voltage margin strongly dependent on exact sampling position
• How do we set the clock at the “best” place?
Conceptual CDR

System Types

• (Source) Synchronous
  • Same frequency & phase

• Mesochronous
  • Same frequency, unknown phase

• Plesiochronous
  • Almost same frequency

* From EE371, Stanford University
Linear (Hogge) Phase Detector

• Edge clock $T_{\text{sym}}/2$ away from data
• Derive early/late from data and edge samples:
  • Dn: $(d_n \neq e_n)$ & $(d_{n-1} \neq d_n)$
  • Up: $(d_n = e_n)$ & $(d_{n-1} \neq d_n)$

Bang-Bang (Alexander) Phase Detector

• Edge clock $T_{\text{sym}}/2$ away from data
• Derive early/late from data and edge samples:
  • Dn: $(d_n \neq e_n)$ & $(d_{n-1} \neq d_n)$
  • Up: $(d_n = e_n)$ & $(d_{n-1} \neq d_n)$