1. **Pole-Zero Doublets:** In this problem we will be looking at the behavior of the pseudo-differential amplifier shown below to gain some intuition into the origin and response of pole-zero doublets. You can assume that $M_1$ and $M_2$ form a differential pair (i.e. their small signal model parameters are identical) with infinite small-signal output impedance ($r_o$). Moreover, you can assume that $R_1$ is larger than $R_2$, and all capacitors are negligible with the exception of the ones explicitly drawn in the diagram.

![Pseudo-differential amplifier circuit diagram](image)

a. Derive an expression for the transfer functions $H_{11}(s) = \frac{V_{o1}(s)}{V_{i1}(s)}$ and $H_{22}(s) = \frac{V_{o2}(s)}{V_{i2}(s)}$ in terms of $R_1$, $R_2$, $C$ and the transistors’ $g_m$.

b. Sketch the magnitudes of $H_{11}$ and $H_{22}$ versus frequency on the same plot.

c. Now derive and sketch the time-domain voltage response of $V_{o1}$ to a voltage step on $V_{i1}$. Similarly, derive and sketch the time-domain voltage response of $V_{o2}$ to a voltage step on $V_{i2}$.

d. Using the results from part a. and part b., sketch the magnitude of the transfer function for differential gain $H(s) = \frac{(V_{o2}-V_{o1})}{(V_{i1}-V_{i2})}$.

e. Now sketch the time-domain voltage response of the differential output $V_{o2}-V_{o1}$ to a differential voltage step $(V_{i1}-V_{i2})$. While you can certainly derive this response using inverse Laplace transforms and partial fractions, you may find it significantly easier to use your answers from the previous sections instead.
2. **Switched-capacitor amplifier:** What is the total noise variance at the output of the switched capacitor amplifier shown below at the end of a complete cycle (i.e., during $\phi_2$)? You can assume that the OTA is simply implemented by an NMOS common-source stage with a given $g_m$ and infinite $r_o$.

![Switched-capacitor amplifier diagram]

3. **Gain Boosted Cascode:** This problem will focus on the gain-boosted cascode amplifier shown below. To simplify the analysis, you can ignore the $r_o$ of the transistors and all of the capacitors except for those explicitly drawn in the diagram.

![Gain Boosted Cascode diagram]

a. What is the frequency response $H(s) = v_3(s)/v_1(s)$ of this amplifier? Approximately what is the unity gain frequency of the amplifier?

b. Approximately what conditions are required to guarantee that the gain boosting feedback loop maintains at least 45° of phase margin? You should provide your answer in terms of $g_{m1}$, $g_{m2}$, $g_{m3}$, $C_1$, $C_2$, and $C_3$. What conditions would we obtain if at least 60° of phase margin are required instead?

c. Assuming this amplifier is used in unity gain feedback, what conditions are required to guarantee that the gain boosting feedback loop does not introduce any significant pole-zero doublets that might limit the settling response?

d. Assume now that $C_1=C_3=50$ fF, $C_2=1.5$ pF, $V^*_M1 = 180$ mV, and $V^*_M2 = 90$ mV. In order to achieve at least 60° phase margin and the criteria from part c), what are the minimum and maximum $g_{m3}/g_{m1}$?