This is an individual assignment!
The goal of this assignment is to get familiar with the class technology. It is fairly long – knowledge of some scripting language (like Perl) could be useful.

1. Spice models
Use the BSIM4 (HSPICE Level 54) model to characterize a predictive 45nm CMOS process; parameter files are at http://www.eas.asu.edu/~ptm/, also on the class home page.

a) Determine the threshold voltage $V_{TH}$, for the NMOS and PMOS devices (for $V_{BS} = 0$, $L = 45$nm and $W = 1\mu$m), by extrapolating from the $I_D-V_{GS}$ curve at low $V_{DS}$. Explain your circuit setup. How does this result compare to values reported in the model file and the DC OP analysis? Also, determine the body-effect parameter.

Circuit Setup: Source of NMOS (or PMOS) tied to gnd (or vdd). Voltage sources Vgs, Vds, and Vsb connected between gate of FET and Source nodes. $V_{DS} = 50mV$, $V_{SB} = 0V$, Vgs DC sweep.

From the table we see that extrapolation matches .OP for PMOS but not for NMOS. In the model file there is $V_{TH}$ which is long channel voltage @ low Vds which is 0.466V for NMOS and -0.4118V for PMOS.
To determine the body effect parameter measure Vth @ different Vbs and extract γ using the equation:

\[ Vt = Vt0 + \gamma \left( \sqrt{(V_{bs} + 2\phi_b)} - \sqrt{2\phi_b} \right) \]

From modelcard, the doping (NDEP) for both PMOS and NMOS is about 1e18 cm\(^{-3}\) which yields

\[ 2\phi_b = (\phi_b + 0.45) = 0.95 \]

Vth is plotted vs different Vbs and γ is extracted using the above equation as shown below:

**NMOS**

![NMOS Graph]

**PMOS**

![PMOS Graph]

The calculated body factor for NMOS is 0.428 while K1 parameter in modelcard is 0.4.
The calculated body factor for PMOS is 0.336 while K1 parameter in modelcard is 0.4.
b) Determine the subthreshold slope factor $S$ for the NMOS and PMOS devices (at $|V_{DS}| = 1.0\text{V}$, room temperature). Determine the drain-source leakage currents at $V_{GS} = 0\text{V}$. Determine the gate leakage currents at $|V_{GS}| = 1.0\text{V}$.
Repeat it at a lower temperature $T = 77\text{K}$.

<table>
<thead>
<tr>
<th></th>
<th>Room T</th>
<th></th>
<th>T=77K</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
</tr>
<tr>
<td>Sub-threshold Slope</td>
<td>105mV/dec</td>
<td>120mV/dec</td>
<td>50mV/dec</td>
</tr>
<tr>
<td>$I_d\mid V_{GS}=0, V_{DS}=1$</td>
<td>101.53nA</td>
<td>68.05nA</td>
<td>36pA</td>
</tr>
<tr>
<td>$I_g\mid V_{GS}=1.0, V_{DS}=1$</td>
<td>9.47nA</td>
<td>3.65pA</td>
<td>7.97nA</td>
</tr>
</tbody>
</table>

*note that while calculating $I_d$s: $I_d=I_d-I_g$ need to exclude leakage from drain to gate @ $V_{GS}=0, V_{DS}=1$.

The parameter for sub-threshold slope in modelcard (NFACTOR) for both NMOS and PMOS is 2.1 which yields slope of 126mV/dec. Our fitting shows that PMOS agrees with it but NMOS is away.

In general most of the parameters showed a little deviation for NMOS compared to the PMOS values. Needs to be examined later.

c) Determine the effects of channel length $L$ on the threshold voltage $V_{Th}$ between 40nm to 60nm. Draw $V_{Th}$ of the NMOS and PMOS as a function of $L$ (for $V_{DS} = 1.0\text{V}$ and $0.8\text{V}$). 

![Graph showing NMOS and PMOS Vth vs L]
d) Determine the effects of drain-source voltage $V_{DS}$, on the threshold voltage $V_{Th}$ between 0 and 1.0 V. Draw $V_{Th}$ as a function of $V_{DS}$ (for $L = 45\text{nm}$). Explain your measurement setup. What is the measured DIBL factor?
2. RC modeling of CMOS gates.
The goal is to explore the equivalent RC models of CMOS gates.

a) Resistance from static DC characteristics: By plotting the $I_d-V_{DS}$ characteristic for $V_{GS} = 1.0\text{V}$ using HSPICE, compute the average resistance of the NMOS ($L = 45\text{nm}$, $W = 1\mu\text{m}$) pull-down switch in an inverter during the transition.

b) Determine optimal $W_P/W_N$ for this technology.
c) Using Hspice, plot the $t_{pHL}$ and $t_{pLH}$ for an inverter with fanouts of FO = 1, 2, 4, 8. Use the simulation setup as shown in Fig. 2.b. Each inverter is sized equally, but drives fanout of its copies. Repeat the simulations for a 2-input NAND, and plot $t_{pHL}$ and $t_{pLH}$. Use 10-90% rise times at the inputs of 20ps, and the optimal $W_P$ with $W_N = 1\mu m$. Find the logical effort of a NAND from these simulations.

Logical effort = 1.33
d) Analytically derive the inverter delay dependence on the input slope. Assume simplest model – where the drain current is linearly proportional to $V_{GS}$.
e) Let’s try to estimate equivalent resistance and capacitance of an inverter during switching, using the setup from Fig. 2.b. Replace the output load of the second inverter in the chain with a capacitor. Determine the capacitance $C_{\text{eff}}$ that results in the same average delay for this inverter as a fanout-of-4 loading inverter. Normalize the input capacitance to a 2μm/1μm inverter. Then, with this linear capacitor in place, find the equivalent output resistance of the first inverter, $R_{\text{eff}}$, that results in the same average delay during switching, and compare this result to value obtained in part a). Comment on possible differences. How could you distinguish the impact of gate and diffusion capacitances?

$$C_{\text{eff}} = 18.5\text{fF}$$

Equivalently, a 2μm/1μm inverter has an input gate $C_{\text{eff}}$ of $5.38\text{fF}$

To find $R_{\text{eff}}$, the first inverter was replaced by a resistor whose value was swept to match the FO4 delay.

$$R_{\text{eff}} = 1.2\text{kΩ}$$

This is considerably more than the value above (674Ω). This can be attributed to the fact that this $R_{\text{eff}}$ is calculated with respect to an average delay (tpHL and tpLH) and so it incorporates the effective resistance of the PMOS as well, which was considerably higher. Also, there is no delay caused by the diffusion capacitance of the inverter and thus delay times with this circuit are faster than they were in the case in which we derived the FO4 delay.

In order to characterize gate and diffusion capacitances separately, you could measure the difference in delay between a FO1 inverter and FO2 inverter. This difference is proportional to the gate capacitance of that gate and can be subtracted from the FO1 inverter delay to give you the portion of delay caused by the intrinsic loading of the inverter (diffusion capacitance).
Using SPICE, find the required width \( W \) for the NMOS transistors in Figure 4.b such that the equivalent resistance of the pull-down network is the same as the equivalent resistance of the pull down network in Figure 4.a. Use 3 input configurations:
1. Both inputs \( A \) and \( B \) switch simultaneously
2. \( B = 1 \) and only \( A \) switches
3. \( A = 1 \) and only \( B \) switches

Report the corresponding \( W \) for each of the 3 situations. Explain your results – compare them with hand analysis. The technology is 1-V 45nm with minimum channel lengths.

**Case 1: Both inputs A and B switch simultaneously (stacked node charged)**
Case 2: B=1 and only A switches

Case 3: A=1 and only B switches

<table>
<thead>
<tr>
<th>Case</th>
<th>Required Width (tp_HL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>2.38um</td>
</tr>
<tr>
<td>Case 2</td>
<td>1.90um</td>
</tr>
<tr>
<td>Case 3</td>
<td>2.00um</td>
</tr>
</tbody>
</table>

These results make intuitive sense. Case 1 and Case 3 require the wider transistors because, in the worst case conditions, the stacked node between the two NMOS is charged to Vdd-Vth. Not only does this add an extra delay time to discharge, it also lowers the initial drive of the NMOS stack because the top NMOS has a very weak Vgs-Vt. Case 1 is slower than Case 3 because of the extra capacitive coupling from the input signal A switching, as can be observed in the overshoot of the first plot.

In the best case, Case 2, both transistors are able to pull large currents (large Vgs-Vt). In terms of sizing, the nand has an equivalent inverter ratio of 2um:1.27um (sized up from the minimum optimal 1.58um:1um inverter) Because of velocity saturation, as seen in the hand analysis, the NMOS only needs to be upsized by ~ 1.5 in a stack. In our case, this means a required width of 1.5*1.27um = 1.898um. This matches very closely with the simulated value of 1.9um
4. **Alpha-power law model**

Let’s examine the alpha power law for the drain current in 1-V 45nm technology using \( L = 45\text{nm} \):

\[
I_D = K(V_{GS} - V_{Th})^\alpha
\]

a) We will try to extract the parameters \( V_{Th} \) and \( \alpha \) from SPICE simulations. Assume \( W_N = 1\mu m, \ W_P = 2\mu m \) and get 10-15 simulation points. Use then Matlab to determine \( K, V_{Th} \) and \( \alpha \) (hint: use the `lsqcurvefit` function). Determine the parameters for both NMOS and PMOS transistors.

\[
\begin{align*}
\text{NMOS} & \quad K = 0.0017 & |K| = 0.0015 \\
& \quad V_{th} = 0.2807 \text{ V} & |V_{th}| = 0.2985 \text{ V} \\
& \quad \alpha = 1.0881 & \alpha = 1.1062
\end{align*}
\]

b) By setting \( \alpha = 1 \), find the \( V_{Th} \) that corresponds to linear dependence of current on \( V_{GS} \).

\[
\begin{align*}
\alpha = 1: \\
\text{NMOS} & \quad K = .0018 \quad V_{thz} = .3155 \text{V} \\
\text{PMOS} & \quad |K| = .0016 \quad |V_{thz}| = .3348 \text{V}
\end{align*}
\]

c) Using the alpha power law model, find the analytical expression for the delay of a CMOS inverter driving a capacitive load. Using the setup as in Problem 2, extract new values of parameters \( V_{Th} \) and \( \alpha \) that fit the best your analytical model for delay. How do they compare to parameters extracted from current fitting?
In order to get points for curve fitting, either Vdd or Cl could be swept (see hand analysis) Since sweeping Cl would give some discrete error (due to intrinsic capacitances), Vdd was swept from .7V to 1.2V

Matlab code:

```matlab
function F = apm(wxyz,x)
    F = 10^15*wxyz(1)*.69*3/4*x./(wxyz(2)*(x-wxyz(3)).^wxyz(4));

XN = LSQCURVEFIT(@apm, [5e-15 1.7e-3 .2807 1.0881],vdd,tplhfix)
XP = LSQCURVEFIT(@apm, [5e-15 1.7e-3 .2807 1.0881],vdd,tplhfix)

K    = 9.62e-4
|K|    = 0.00244
Vth   = 0.408 V
|Vth|   = 0.3635 V
α     = 1.38
α     = 1.1776
```

The values extracted are similar to the values extracted from the current fitting.