1. **Circuit Setup**

![Circuit Diagram]

(a) We use \( V_{ds} = 50 \text{mV} \). \( V_{gs} \) is swept from 0 to 1 V and \( I_{ds} \) is measured.

See attached graph Fig 1 & Fig 2.

For NMOS, extrapolated \( U_{th} = 658.6 \text{mV} \):

- Model file \( U_{th} = \frac{658.6 \text{mV}}{2} = 329.3 \text{mV} \)
- \( 0 \text{p} \) \( U_{th} = 681.9734 \text{mV} \)

For PMOS, extrapolated \( U_{th} = 638 \text{mV} \):

- Model file \( U_{th} = 637.45 \text{mV} \)
- \( 0 \text{p} \) \( U_{th} = 624.4590 \text{mV} \)

(b) Set-up similar to (a). However, \( V_{gs} \) is swept from 0 to 0.6 V. \( V_{ds} = 0.5 \text{V} \)

See attached graph Fig 3 & Fig 4.

For NMOS, sub-threshold slope factor \( S = 89.1856 \text{mV/dec} \):

\[
I_{ds}(V_{gs} = 0) = 608.74 \text{pA} \quad 20.4 \text{pA}
\]

For PMOS, sub-threshold slope factor \( S = 89.32 \text{mV/dec} \):

\[
I_{ds}(V_{gs} = 0) = 359.44 \text{pA} \quad 21.4 \text{pA}
\]

(c) Graph of leakage current vs. length: See Figure 5.86

As expected, the leakage current increases exponentially as \( L \) is decreased.

Graph of threshold voltage vs. length: See Figure 7.88

As expected, the threshold voltage increases with length.
(d) Use the same setup as before, sweep $V_{Tn}$ from 0 to 0.85 V and plot $I_{Th}$.
See Figure 98.10 for the plot.

From the graph, the DIBL factor for NMOS is $-0.132 \ \text{V/\mu}$
For MOS is $-0.150$

2 (a) For NMOS, MATLAB fit result is
$$I_p = \frac{0.00485 \times 0.721 \times (V_{gs} - 0.492)^2}{(V_{gs} - 0.992) + 0.721}$$
$$E_{cL} = 0.721 \ \text{V}$$
For NMOS, MATLAB fit result is
$$I_p = \frac{0.00485 \times 0.721 \times (V_{gs} - 0.492)^2}{(V_{gs} - 0.992) + 0.721}$$
$$E_{cL} = 0.721 \ \text{V}$$
See attached plots. Fig. 11 & 12

(b) With $E_{cL} = 0.498 \ \text{V}$, saturation occurs at
$$V_{DS} = \frac{(V_{gs} - V_{Tn}) E_{cL}}{(V_{gs} - V_{Tn}) + E_{cL}}$$
See attached graph. Fig. 13

(c) For NMOS, MATLAB fit result is
$$I_p = 0.00174 \times (V_{gs} - 0.5488)^{1.32}$$
$$K = 0.00174 \ , \ V_{Tn} = 0.5488 \ \text{V} \ , \ \alpha = 1.32$$
For PMOS, MATLAB fit result is
$$I_p = 0.001436 \times (V_{gs} - 0.5198)^{1.355}$$
$$K = 0.001436 \ , \ V_{Tn} = 0.5198 \ \text{V} \ , \ \alpha = 1.355$$
See attached graphs. Fig. 14 & 15
d. With \( d = 1 \), for NMOS, the \( V_{th} \) is \( 0.5946 \) \( V \) \((K=0.06)\).

For PMOS, the \( V_{th} \) is \( 0.5788 \) \( V \) \((K=0.06)\).

See attached figure 16 & 17.

(take + take) / 2 is measured and plotted (see attached) From graph, \( \beta \) is \( 1.17 \) for minimum average delay.

See attached figure 18.

\[(6)\]

Equivalent to \( \text{composite cross section} \):

\[
\frac{w}{l} \Rightarrow \frac{w}{2l}
\]

\[
V_{sat} = \frac{(V_{gs} - V_{T})E_c(2L)}{(V_{gs} - V_{T}) + E_c(2L)}
\]

\[
= \frac{(0.95 - 0.4) \times 2 \times 0.8}{(0.95 - 0.4) + 2 \times 0.8} = 0.4093 \, V
\]

\[
V_{sat} = 0.4093 < V_{dd} = 0.935 \rightarrow \text{the transistors is velocity limited}
\]

\[
I_{diss} \text{ (composite)} = \frac{I_{diss} \text{ (NMOS)} + I_{diss} \text{ (PMOS)}}{2}
\]

\[
1 \times V_{sat} C_{ox} \frac{(V_{gs} - V_{th})^2}{(V_{gs} - V_{th}) + E_c} = \frac{W \times V_{sat} C_{ox} (V_{gs} - V_{th})^2}{(V_{gs} - V_{th}) + E_c} \times \frac{1}{2}
\]

\[
\Rightarrow \omega = \frac{1}{4} \times \frac{(0.95 - 0.4) + 2 \times 0.8}{(0.95 - 0.4) + 0.8} \approx 1.5926 \, \text{\( \checkmark \)}
\]
\[
\frac{1}{\sqrt{2}} \cdot w, L \quad \Rightarrow \quad \frac{1}{\sqrt{2}} \cdot w, 1.5 L
\]

\[
V_{\text{set, linear}} = \frac{(V_{gs} - V_{th}) \cdot 1.5 E_c L}{V_{gs} - V_{th} + 1.5 E_c L}
\]

\[
= \frac{0.95 - 0.9 \times 1.5 \times 0.85}{0.95 - 0.9 + 1.5 \times 0.85} = \frac{0.384}{0.975} = \frac{V_{th}}{V}
\]

\( \Rightarrow \text{velocity saturated} \)

\[
W = \frac{1 \times V_{\text{set,cox}} \times (V_{gs} - V_{th})^2}{(V_{gs} - V_{th}) + \varepsilon_c L} = \frac{W \times V_{\text{set,cox}} \times (V_{gs} - V_{th})^2}{V_{gs} - V_{th} + 1.5 E_c L}
\]

\[
= \frac{0.95 - 0.9 + 1.5 \times 0.85}{0.95 - 0.9 + 0.85} = 1.30357
\]
Fig. 3

NMOS-Ids/A vs Vgs/V in subthreshold

Fig. 4

PMOS-Ids/A vs Vgs/Vin subthreshold
Fig. 5 Graph of Leakage current $I_{ds}/A$ vs Channel Length $/m$ for NMOS

Fig. 6 Graph of Leakage current $I_{ds}/A$ vs Channel Length $/m$ for PMOS
Fig. 7 Graph of Threshold Voltage/V vs Channel Length /m for NMOS

Fig. 8 Graph of Threshold Voltage/V vs Channel Length /m for PMOS
Fig. 9 Graph of Threshold Voltage/V vs Vds/V for NMOS

Fig. 10 Graph of Threshold Voltage/V vs Vds/V for PMOS
Fig. 11 NMOS Graph of $I_d/A_v$ vs $V_{gs}/V$ for real and velocity saturation model

Fig. 12 PMOS Graph of $I_d/A_v$ vs $V_{gs}/V$ for real and velocity saturation model
Fig. 14 NMOS Graph of $I_{ds}/V_{ds} V_{gs}/V$ for real and alpha model

Fig. 15 PMOS Graph of $I_{ds}/V_{ds} V_{gs}/V$ for real and alpha model
Fig. 16 PMOS Graph of $I_{ds}/V_{gs}$ vs $V_{gs}/V$ for real and alpha model with alpha=1

Fig. 17 PMOS Graph of $I_{ds}/V_{gs}$ vs $V_{gs}/V$ for actual and alpha model with alpha=1
Figure 18. Graph of $t_{\text{avg}} \equiv (t_{PL} + t_{LH}) / 2$ vs beta