Problem 1. Sequential elements.  
A sequential element is shown in Figure 1.

![Circuit Diagram](image)

**Figure 1.**

a) Is this circuit a latch or a flip-flop? Explain.
b) What is the difference between a conventional implementation of such a circuit and the proposed implementation from Figure 1? When and why would you use the circuit from Figure 1 instead of the conventional one?


a) Using the alpha-power law model, derive the analytical expression for the energy/delay sensitivity of a design to scaling of a supply voltage. Evaluate this expression at the nominal supply voltage, using the results from Homework 1 ($K = 0.001, \alpha = 1.6, V_{TH} = 0.45V$, for NMOS)
b) What is the energy/delay sensitivity of a design to the logic depth? You can define the logic depth as a number of FO4 inverters that fit into one clock period.

Problem 3. Subthreshold design.
a) From the lecture notes, it appears that, for a design operating in subthreshold, the minimum energy point of a design does not depend on the threshold voltage, and only depends on the supply. Can you explain why (very briefly)?

b) If it doesn’t matter for the energy, why is it important to control the transistor threshold voltage in subthreshold design?