Announcements

- Homework 1 due today
- Quiz #1 next Monday
Outline

- SRAM static margins
- SRAM dynamic margins
- Assist techniques

22nm SRAM

- FinFET cell design

E. Karl, ISSCC'12
SRAM

Static Retention Margin

SRAM Cell/Array

› Hold (retention) stability
› Read stability
› Write stability
› Read current (access time)

Access Transistor

Pull down

Pull up

WL

BL

VDD

M

5

M

6

M

4

M

3

M

2

M

1

M

Q

Access Transistor
SRAM Design – Hold (Retention) Stability

Scaling trend:

- Increased gate leakage + degraded $I_{ON}/I_{OFF}$ ratio
- Lower $V_{DD}$ during standby
- PMOS load devices must compensate for leakage

Retention Stability

Would like to reduce supply in standby
Monte-Carlo Simulation of DRV Distribution

Vmin Distribution

- Alternative to static margin characterization
- Digital test under supply sweep
SRAM

Static Read/Write Margins

6T-SRAM Array Basics – Read Operation

- WL: Word Line
- BL: Bit Line
- BLT: Bit Line Translator
- BLC: Bit Line Coupling
- NC: Node Coupling
- NT: Node Translator
- RBSn: Read Buffer Select
- DLC: Dynamic Logic Coupler
- DOn: Data Out
- SET: Set
- DO: Data Output

- Full-down / Transfer-device ratio (Beta ratio) determines how high the low node rises

H. Pilo, IEDM 2006
Read Stability – Static Noise Margin (SNM)

Read SNM is the contention between the two sides of the cell under read stress.

\[ \Delta V_{th} \propto \frac{1}{C_{ox} \sqrt{WL}} \]

Due to RDF

E. Seevinck, JSSC 1987

Read SNM - Measurements

Read margin vs. retention margin
Bhavnagarwala, IEDM'05
Read Stability – N-Curve

- A, B, and C correspond to the two stable points A and C and the metastable point B of the SNM curve
- When points A and B coincide, the cell is at the edge of stability and a destructive read can occur

Grossar, JSSC’06

6T-SRAM Array Basics – Write Operation

- “Weak” 1 written through source-follower NFET-fer device
- High-node discharged through series stacked NFET devices. NFET effective device strength must overcome cell pull-up.

H. Pilo, IEDM 2006
Write Stability – Write Noise Margin (WNM)

- Writeability is becoming harder with scaling
- Optimizing read stability and writeability at the same time is difficult

A. Bhavnagarwala, IEDM 2005

Write Stability – BL/WL Write Margins

- Highest BL voltage under which write is possible when BLC is kept precharged
- Difference between VDD and lowest WL voltage under which write is possible when both bit-lines are precharged
Write Stability – Write Current (N-Curve)

- Minimum current into the storage node

C. Wann et al, IEEE VLSI-TSA 2005

The Conflict Between Read and Write

READ - OPTIMIZED SYSTEM

WRITE - OPTIMIZED SYSTEM

H. Pilo, IEDM 2006
6-T SRAM Static/Dynamic Stability

- **Read Margin**
  - SNM: pessimistic
- **Write Margin**
  - WNM: optimistic
- Introduction to dynamic margins

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**SRAM**

Dynamic Margins
Dynamic Write Stability

- $T_A < T_{\text{write}} < T_B$
- $T_{\text{write}} =$ dynamic write stability
- Static margins are optimistic

Khalil, TVLSI'08

Dynamic Read Stability

- $T_A < T_{\text{read}} < T_B$
- $T_{\text{read}} =$ dynamic read stability
- Static margins are pessimistic

Khalil, TVLSI '08
Dynamic Read Access

- \( T_A < T_{access} < T_B \)
- \( PD_1 \) and \( PG_1 \) are critical

Khalil, TVLSI '08

V\textsubscript{Th} Window

- Assuming global spread

Yamaoka, ISSCC'05
Peripheral Circuits to Help SRAM

- Write assist techniques
- Read assist techniques
- Redundancy
- ECC
Multi-Voltage SRAM

Array Adjustments

Array back bias, to compensate for systematic variations

S. Mukhopadhyay, VLSI 2006
Dynamic V_{DD} Implementation

- VCC selection is along column direction to decouple the read & write

Zhang, ISSCC'05

Floating VDD Technique

- W/o second supply

Yamaoka, ISSCC'04
Collapsing $V_{DD}$ Technique

Collapsing $V_{DD}$ Technique

E. Karl, ISSCC’12

E. Karl, ISSCC’12
Next Lecture

- Other assist techniques in SRAM
- Redundancy/ECC