EE241 - Spring 2012
Advanced Digital Integrated Circuits

Lecture 11: SRAM Design

Announcements

› Homework 2 due Wednesday, March 14
› Midterm project reports due Wednesday, March 21
› Quiz #1 today
› No lecture on Wednesday
Outline

- ECC techniques in SRAM
- Alternatives to 6T SRAM
- Back to timing

SRAM

Redundancy and ECC
Multi-bit Errors


Kawahara, ISSCC'07 tutorial
Multi-bit Errors

Equivalent circuits of 16 SRAM cells between well tap

Max. no. of errors per cell: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

Nc is the number of cells between well taps.

Multi-bit Errors: Interleaving

Placement at alternate addresses

Multi-error B

Word<0> A1 A1 A1 A1 A1 A1 A1

Word<1> A2 A2 A2 A2 A2 A2 A2

Word<2> A3 A3 A3 A3 A3 A3 A3

Word<3> A4 A4 A4 A4 A4 A4 A4

Word<4> A5 A5 A5 A5 A5 A5 A5

Address-0

Address-1

Data is not corrected

All data is corrected

Neutron peak energy: 63.5 MeV
Total fluency: 6.14 x 10^{10}/cm^{2}

w/o ECC

-99.5%

This work

Ref.: K. Osada et al., [12].

Ref.: K. Osada et al., [11]
SRAM

Options for scaling

Vmin Scaling Projections

Itoh, ISSCC’09
SRAM Scaling

› Approaching fundamental limits:
  › Don’t scale cell size
  › Increase transistor count (from 6)
  › Change technology (e.g. double-gate FETs)
  › eDRAM
  › Or something else…

SRAM Alternatives

8-T SRAM

• Dual-port read/write capability (register file-like cells)
• N0, N1 separates read and write
  • No Read SNM constraint
  • Half-selected cells still undergo read stress – no single cell write capability
• Stacked transistors reduce leakage

L. Chang, VLSI Circuits 2005
Alternatives: Thin-Body MOSFETs

- Thin body suppresses short channel effects
  - Channel lightly doped $\rightarrow$ higher carrier mobility
  - $T_{ox}$ scaling not needed $\rightarrow$ less reliability issues
- Double-gate structure is scalable to $L_g<10$nm

![Double-Gate (DG) and Ultra-Thin Body (UTB)]

6-FinFET SRAM Cell

![6-FinFET SRAM Cell Diagram]

175mV SNM w/ 0.36$\mu$m$^2$ cell area
6-FinFET SRAM Cell: 2 Fins

240mV SNM w/ 0.42μm² cell area
36% SNM improvement w/ 17% area penalty

Bulk-Si FinFETs

FinFETs can be made on bulk-Si wafers
✓ lower cost
✓ improved thermal conduction to mitigate self-heating effects
✓ integration with planar bulk-Si MOSFETs is possible

Lee, VLSI'04, Kavaleros, VLSI'06
eDRAM

- Process cost: Added trench capacitor

Barth, ISSCC '07, Wang, IEDM '06

Timing
Latch Parameters

Delays can be different for rising and falling data transitions

Flip-Flop (Register) Parameters

Delays can be different for rising and falling data transitions
Clock Nonidealities

- Clock skew
  - Spatial variation in temporally equivalent clock edges; deterministic + random, $t_{\text{SK}}$
- Clock jitter
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
  - Cycle-to-cycle (short-term) $t_{\text{JS}}$
  - Long term $t_{\text{JL}}$
- Variation of the pulse width
  - for level sensitive clocking
Clock Skew and Jitter

- Both skew and jitter affect the effective cycle time
- Only skew affects the race margin, if jitter is from the source
  - Distribution jitter affects both

Clock Uncertainties

Sources of clock uncertainty
Clock Constraints in Edge-Triggered Systems

Next Lecture

- Latch-based timing