Announcements

- Homework #2 due on Friday (in BWRC)
- Midterm project reports due Wednesday, March 21
- Quiz #2 on March 19
Outline

- Timing revisited
- Latch-based timing

Timing
Latch-Based Timing

As long as transitions are within the assertion period of the latch, no impact of position of clock edges.

Latch Design and Hold Times
Latch-Based Timing

- Longest path
  \[ T_{CY} \geq 2T_{DQM} + T_{LHM} + T_{LLM} \]

  Independent of skew

- Short paths
  \[ T_{CLLm} \geq T_{SK} + T_H - T_{CQm} \]
  \[ T_{CLHm} \geq T_{SK} + T_H - T_{CQm} \]

  Same as register-based design but holds for both clock edges

Can tolerate skew!
Soft-Edge Properties of Latches

- Slack passing – logical partition uses left over time (slack) from the previous partition
- Time borrowing – logical partition utilizes a portion of time allotted to the next partition
- Makes most impact in unbalanced pipelines

Bernstein et al, Chapter 8, Chandrakasan, Chap 11 (by Partovi)

Slack-Passing and Cycle Borrowing

For N stage pipeline, overall logic delay should be < N \( T_{cl} \)
Latches: Reading

- Rabaey et al, Chapters 7 and 10
- Chapter 10 in Chandrakasan et al, by Partovi
- Stojanovic, Oklobdzija, JSSC 4/99
Latch vs. Flip-Flop

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Latch Pair vs. Flip-Flop

- **Performance metrics**
- **Delay metrics**
  - Delay penalty
  - Clock skew penalty
  - Inclusion of logic
  - Inherent race immunity
- **Power/Energy Metrics**
  - Power/energy
  - PDP, EDP
- **Design robustness**
Latches

Transmission-Gate Latch

C powdered MOS Latch

(a) The transparent high latch (THL)

(b) The transparent low latch (TLL)

(c) Timing waveforms for the THL

*Courtesy of IEEE Press, New York. © 2000*
Latch Pair as a Flip-Flop

Requirements for the Flip-Flop Design

- High speed of operation:
  - Small Clk-Output delay
  - Small setup time
  - Small hold time—Inherent race immunity
- Low power
- Small clock load
- High driving capability
- Integration of logic into flip-flop
- Multiplexed or clock scan
- Robustness
Sources of Noise

1. Noise on input
2. Leakage
3. α-Particle and cosmic rays
4. Unrelated signal coupling
5. Power supply ripple


Types of Flip-Flops

Latch Pair (Master-Slave)

Pulse-Triggered Latch
Flip-Flop Delay

Sum of setup time and Clk-output delay is the true measure of the performance with respect to the system speed

\[ T = T_{Clk-Q} + T_{Logic} + T_{setup} \] (ignoring skew)

Delay vs. Setup/Hold Times

[Graph showing data-clk vs. clk-output with minimum data-output, setup, and hold points.]
Master-Slave Latch Pairs

Case 1: PowerPC 603 (Gerosa, JSSC 12/94)

![Master-Slave Latch Diagram]

Master-Slave Latches

Case 2: C²MOS

Feedback added for static operation
Locally generated clock
Poor driving capability
Pulse-Triggered Latches

- First stage is a pulse generator
  - generates a pulse (glitch) on a rising edge of the clock
- Second stage is a latch
  - captures the pulse generated in the first stage
- Pulse generation results in a negative setup time
- Frequently exhibit a soft edge property

- Note: power is always consumed in the pulse generator

Pulsed Latch

Simple pulsed latch

Kozu, ISSCC’96
Intel/HP Itanium 2

Pulse-Triggered Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC'96
HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time

Hybrid Latch Flip-Flop

Skew absorption

Partovi et al, ISSCC’96
Pulse-Triggered Latches

Semi-Dynamic Flip-Flop (SDFF),
Sun UltraSparc III, Klass, VLSI Circuits'98

Pulse generator is dynamic, cross-coupled latch is added for robustness. Loses soft edge on rising transition
Latch has one transistor less in stack - faster than HLFF, but 1-1 glitch exists
Small penalty for adding logic
Pulse-Triggered Latches

7474, from mid-1960’s

First stage is a sense amplifier, precharged to high, when \( \text{Clk} = 0 \)
After rising edge of the clock sense amplifier generates the pulse on \( S \) or \( R \)
The pulse is captured in S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges
Sense Amplifier-Based Flip-Flop

Sampling Window Comparison

Naffziger, JSSC 11/02
Next Lecture

» Power-performance tradeoffs