Outline

- Features of modern technologies
  - Lithography
  - Process technologies
Lithography and Its Implications

Litho: How to Enhance Resolution?

1. Immersion
2. Off-axis illumination
3. Resolution enhancement/Optical proximity correction
4. Restricted design rules (RDR)
5. Phase-shifting masks
6. Double patterning
1. Immersion

- Project through a drop of liquid
- \( n_{\text{water}} = 1.47 \)

\[
CD_{\text{min}} = k_1 \frac{\lambda}{NA} = 0.25 \frac{193 \text{nm}}{1.35} = 35 \text{nm}
\]

2. Illumination

- Regular Illumination
- Many off-axis designs (OAI)
  - Annular
  - Quadrupole / Quasar
  - Dipole
- Amplifies certain pitches/rotations at expense of others

A. Kahng, ICCAD'03
3. Resolution Enhancement

J. Hartmann, ISSCC'07

 OPC

Optical Proximity Correction (OPC) modifies layout to compensate for process distortions

- Add non-electrical structures to layout to control diffraction of light
- Rule-based (past) or model-based

Design → OPC → Fracture → Mask

A. Kahng, ICCAD'03
4. Restricted Design Rules

- 45nm technology example

Also: note poly density rules

J. Hartmann, ISSCC'07

5. Phase-Shift Masks

- Phase Shifting Masks (PSM)
  - Creates interference fringes on the wafer → Interference effects boost contrast → Phase Masks can make extremely small lines

conventional mask

phase shifting mask

A. Kahng, ICCAD'03
Litho: Current Options (22nm)

- **Immersion lithography**
  - Use high index (NA ~ 1.6-1.7, $k_1 < 0.3$)

- **Double patterning**
  - NA ~ 1.2-1.35

- **EUV lithography (?)**
  - $\lambda = 13.5\text{nm}$

6. Double Patterning

- **Double exposure double etch**
  - Double exposure double etch
  - Pitch split

- **Double exposure single etch**
  - Dipole decomposition (DDL)
  - Pack-unpack for contact
  - Resist freeze technology
  - Sidewall image transfer (SIT)

From Colburn, VLSI Technology 2008 Workshop
Double-Exposure Double-Etch

Starting layout

Line + cut split

Cut over line

Result:

SRAM image from K. Mistry, IEDM'07

Pitch Split Double Exposure

Starting layout

Split pattern

Overlay

With overlay misalignment
### 32nm Examples

**Single exposure**

**Double exposure**

[IEDM'08](#)

### Litho: Design Implications

- **Forbidden directions**
  - Depends on illumination type
  - Poly lines in other directions can exist but need to be thicker

- **Forbidden pitches**
  - Nulls in the interference pattern

- **Forbidden shapes in PSM**

- **Assist features**
  - If a transistor doesn’t have a neighbor, let’s add a dummy
Technology Features

Technology features

1. Shallow-trench isolation
2. High-k/Metal-gate technology
3. Strained silicon
4. Thin-body devices
5. Copper interconnects with low-k dielectrics
1. Shallow Trench Isolation

- Less space needed for isolation
- Some impact on stress

2. Hi-k/Metal gate

Gate leakage can be improved by 4 decades by using High-K/Metal Gate Stack

TEM X-section of HighK/Metal Gate Stack on FDSOI

Replacement gate technology (Intel)

S. Natarajan, IEDM’08
3. Strained Silicon

Compressive channel strain
30% drive current increase
in 90nm CMOS

Tensile channel strain
10% drive current increase
in 90nm CMOS

Intel’s Strained Si Numbers

Performance gains:

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<th>90 nm</th>
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<th>65 nm</th>
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<td></td>
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S. Thompson, VLSI’06 Tutorial
4. Thin-Body MOSFET Structures

- Thin body suppresses short channel effects
  - Channel lightly doped → higher carrier mobility
  - $T_{ox}$ scaling not needed → less reliability issues
  - Double-gate structure is scalable to $L_g<10\text{nm}$
Double-Gate “FinFET”

Planar Double-gate FET

(90° rotation)

FinFET

- Rotation allows for self-aligned gate electrodes
- FinFET layout is similar to that of a planar FET

D. Hisamoto et al., IEDM 1998
N. Lindert et al., IEEE EDL, 2001

Double-Gate vs. Tri-Gate

Double-gate

\[ W = 2H_{FIN} \]

- High device currents per area/layout density
- Requires contacts to fins and narrow fin pitch

Tri-gate

\[ W = 2H_{FIN} + \alpha T_{Si} \]

B. Doyle et al., VLSI, 2003
Sub-5nm FinFET

Alternative: Extremely Thin SOI

Thin-Body SOI MOSFET

SOI: Silicon-on-Insulator

Cheng, IEDM’09
5. Interconnect

Interconnect: CMP

Cu interconnect: Dual damascene process

- Ta barrier layer to prevent Cu from diffusing into Si
- Etch stop (SiN)

Metal density rules (20%-80%)
Slotting rules
Next Lecture

› Device models