EE241 - Spring 2012
Advanced Digital Integrated
Circuits

Lecture 4: Transistor Models

Outline

- Features of modern technologies
  - Finish with device options
- Transistor modeling
Technology Features

Technology features

1. Shallow-trench isolation
2. High-k/Metal-gate technology
3. Strained silicon
4. Thin-body devices
5. Copper interconnects with low-k dielectrics
4. Thin-Body MOSFET Structures

- Thin body suppresses short channel effects
  - Channel lightly doped → higher carrier mobility
  - $T_{ox}$ scaling not needed → less reliability issues
- Double-gate structure is scalable to $L_g < 10\text{nm}$

![Ultra-Thin Body (UTB) and Double-Gate (DG) examples]

**Double-Gate “FinFET”**

- Rotation allows for self-aligned gate electrodes
- FinFET layout is similar to that of a planar FET

![Planar Double-gate FET and 90° rotated FinFET examples]

D. Hisamoto et al., *IEDM*, 1998
N. Lindert et al., *IEEE EDL*, 2001
Double-Gate vs. Tri-Gate

Double-gate
\[ W = 2H_{\text{FIN}} \]

- High device currents per area/layout density
  - Requires contacts to fins and narrow fin pitch

Tri-gate
\[ W = 2H_{\text{FIN}} + \alpha T_{\text{Si}} \]

B. Doyle et al., VLSI, 2003

Sub-5nm FinFET


Lee, VLSI Technology, 2006
Alternative: Extremely Thin SOI

Thin-Body SOI MOSFET

SOI: Silicon-on-Insulator

Cheng, IEDM’09

FinFET Design Issues

- Discrete (quantized) sizing
- Layout compatibility

See Ludwig et al, SOI'03
5. Interconnect

Interconnect: CMP

Cu interconnect: Dual damascene process

- Ta barrier layer to prevent Cu from diffusing into Si
- Etch stop (SiN)

- Metal density rules (20%-80%)
- Slotting rules
Device Models

- Transistor models
  - I-V characteristics
  - C-V characteristics
- Interconnect models
  - R, C, L
  - Covered in EE141
Transistor Modeling

- Different levels:
  - Hand analysis
  - Computer-aided analysis (e.g. Matlab)
  - Switch-level simulation (e.g. NanoSim)
  - Circuit simulation (Hspice)
- These levels have different requirements in complexity, accuracy and speed of computation
- We are primarily interested in delay and energy modeling, rather than current modeling
- But we have to start from the currents

Transistor Modeling

- DC
  - Accurate I-V equations
  - Well behaved conductance for convergence (not necessarily accurate)
- Transient
  - Accurate I-V and Q-V equations
  - Accurate first derivatives for convergence
  - Conductance, as in DC
- Physical vs. Empirical

BSIM group
Transistor I-V Modeling

- BSIM
  - Superthreshold and subthreshold models
  - Need smoothening between two regions
- EKV/PSP
  - One continuous model based on channel surface potential

MOS I-V (BSIM)

Start with the basics:

\[ I_{DS} = WC_{ox}(V_{GS} - V_{Th} - \mu E) \]

\[ I_{DS} = WC_{ox}(V_{GS} - V_{Th} - \mu E) \left( \frac{dV_{C}(x)}{dx} \right) \]

- When integrated over the channel:

\[ I_{DS} = \frac{W}{L} \mu C_{ox} \left( V_{GS} - V_{Th} - \frac{V_{DS}}{2} \right) V_{DS} \]

- Transistor saturates when \( V_{GD} = V_{Th} \) - the channel pinches off at drain’s side.

\[ I_{DS} = \frac{W}{2L} \mu C_{ox} \left( V_{GS} - V_{Th} \right)^2 \]
MOS Currents (0.13μm CMOS with L>>1μm)

Currents according to the quadratic model
Correct for long channel devices (L ~ μm)

Simulated 0.13μm Transistor

L = 0.13μm
Simulation vs. Model

Major discrepancies:
- shape
- saturation points
- output resistances

Velocity Saturation

\[ E_C = \frac{v_{sat}}{\mu_{eff}} \]

\[ v_{sat} = 10^5 \]

Constant velocity

Constant mobility (slope = \( \mu \))
Modeling Velocity Saturation

Fit the velocity-dependence curve

\[ v = \frac{\mu_{\text{eff}} E}{n E_c} \left(1 + \left(\frac{E}{E_c}\right)^n\right)^{1/n} \]

NMOS: \( n = 2 \)
PMOS: \( n = 1 \)

A few approximations: \( n \to \infty \), \( n = 1 \), piecewise
**Approximation** \( n \to \infty \)

1) \( v = \mu_{eff} E, \ E < E_c \)

\[
I_{DS} = \frac{\mu_C W}{L} \left( (V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2} \right)
\]

2) \( v = v_{sat}, \ E > E_c \)

\[
I_{Dsat} = \frac{\mu_C W}{L} \left( (V_{GS} - V_{th})V_{Dsat} - \frac{V_{Dsat}^2}{2} \right)
\]

\( V_{dsat} = ? \)

Can be reduced to EE141 model by \( V_{Dsat} = \text{const} \)

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**MOS Models**

\[
I_D = 0 \quad \text{for} \quad V_{GT} \leq 0
\]

\[
I_D = k \frac{W}{L} \left( V_{GT}V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS}) \quad \text{for} \quad V_{GT} \geq 0
\]

with \( V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}) \),

\[
V_{GT} = V_{GS} - V_T
\]

and

\[
V_T = V_{T0} + \gamma (\sqrt{-2\phi_F} + V_{SB} - \sqrt{-2\phi_F})
\]

\( \gamma \) - body effect parameter

From EECS141

Rabaey, 2nd ed.
Unified MOS Model

- Model presented is compact and suitable for hand analysis.
- Still have to keep in mind the main approximation: that $V_{DSat}$ is constant. When is it going to cause largest errors?
  - When $E$ scales – transistor stacks.
  - But the model still works fairly well.

Approximation $n = 1$, piecewise

- $n = 1$ is solvable, piecewise closely approximates

$$v = \begin{cases} \frac{\mu_{eff} E}{1 + E/E_0}, & E < E_0 = \frac{2v_{sat}}{\mu_{eff}} \\ v_{sat}, & E > E_0 \end{cases}$$

Sodini, Ko, Moll, TED’84
Toh, Ko, Meyer, JSSC’88
BSIM model
Drain Current

We can find the drain current by integrating

\[ I_{DS} = W C_{ox} (V_{GS} - V_{Th} - V_D(x)) v \]

\[ I_{DS} = \frac{\mu C_{ox}}{1 + (V_{DS}/E_C L)} W \left( (V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2} \right) \]

In saturation:

\[ I_{DSat} = C_{ox} W_{sat} (V_{GS} - V_{Th} - V_{Desat}) \]

\[ I_{Desat} = \frac{\mu C_{ox}}{1 + (V_{Desat}/E_C L)} W \left( (V_{GS} - V_{Th}) V_{Desat} - \frac{V_{Desat}^2}{2} \right) \]

Drain Current in Velocity Saturation

Solving for \( V_{Desat} \)

\[ V_{Desat} = \frac{(V_{GS} - V_{Th})E_C L}{(V_{GS} - V_{Th}) + E_C L} \]

And saturation current

\[ I_{DSat} = \frac{W \mu_{eff} C_{ox} E_C L}{2 \left( V_{GS} - V_{Th} \right)^2} \left( V_{GS} - V_{Th} \right) + E_C L \]
Drain Current

![Graph of Drain Current](image)

### Velocity Saturation

- In 0.13\(\mu\)m technology, \(E_C L\) is about \(0.5V_{GS} + 0.7V\)
- Can calculate \(V_{DSat}\) (\(V_{Th} \sim 0.25V\))

<table>
<thead>
<tr>
<th>(V_{GS} [V])</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
<th>1.0</th>
<th>1.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{DSSat} [V])</td>
<td>0</td>
<td>0.13</td>
<td>0.26</td>
<td>0.37</td>
<td>0.46</td>
<td>0.55</td>
</tr>
</tbody>
</table>

- For \(V_{GS} - V_{Th} \ll E_C L\), \((V_{GS} < 1V)\)
  - \(V_{DSat}\) is close to \(V_{GS} - V_{Th}\)
- For large \(V_{GS}\), \(V_{DSat}\) would start bending upwards toward \(E_C L\), but we won’t even notice it with 1.2V supply.
- Therefore \(E_C L\) can be frequently approximated with a constant term (\(E_C L = 1.2V\) in 0.13\(\mu\)m)
Application of Models: NAND Gate

2-input NAND gate

Sizing for equal transitions:
• P/N ratio (β-ratio) of 1.6 about
• Upsizing stacks by a factor proportional to the stack height
Transistor Stacks

- With transistor stacks, $V_{DS}$, $V_{GS}$ reduce.
- Unified model assumes $V_{DSat} = \text{const}$.
- For a stack of two, appears that both have exactly double $R_{on}$ of an inverter with the same width.
- Therefore, doubling the size of each, should make the pull down $R$ equivalent to an inverter.

Velocity Saturation

- As $(V_{GS} - V_{Th})/ECL$ changes, the depth of saturation changes.

$$I_{DSat} = \frac{W}{L} \mu_{\text{eff}} C_{ox} \frac{E_C L}{2} \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L}$$

- For $V_{GS}, V_{DS} = 1.2V, E_C L$ is $1.3V$.
- With double length, $E_C L$ is $2.6V$ (in this model).
- Stacked transistors are less saturated.
- $V_{GS} - V_{Th} = 0.95V$, $I_{DSat} \sim 2/3$ of inverter $I_{DSat}$ (63%).
- Therefore NAND2 should have pull-down sized 1.5X.
- Check any library NAND2’s.
Velocity Saturation

› How about NAND3?
› $I_{DSat} = 1/2$ of inverter $I_{DSat}$ (instead of 1/3)
› How about PMOS networks?
› NOR2 – 1.8x, NOR3 – 2.4x
› What is $E_{C,L}$ for PMOS?

Next Lecture

› Continue transistor modeling, capacitance, leakage
› Delay modeling