Use the SPICE model to characterize the class 32nm LP CMOS process; parameter files correspond to devices n105 and p105 in the process directory (~ee241/synopsys-32nm/hspice/saed32nm.lib, use hspice). The nominal supply voltage for this process is 1.05V. Note that the devices need to be instantiated as subcircuits in SPICE (Use an X prefix, not M).

1. Models

a) Determine the threshold voltage $V_{Th}$, for the NMOS and PMOS devices (for $V_{BS} = 0$, $L = 32\text{nm}$ and $W = 1\mu\text{m}$), by extrapolating from the $I_D-V_{GS}$ curve at low $V_{DS}$. Explain your circuit setup. How does this result compare to values reported in the model file and the DC OP analysis?

b) For the model used in class $I_{DSat} = \frac{W}{L} \mu_{eff} C_{ox} E_C L \left(\frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_C L}\right)$, find the values of $E_C L$ that best fit the NMOS and PMOS characteristics. Use the $V_{Th}$ value from part a). Note that you may want to modify the $I_{Dsat}$ equation to account for finite output resistance.

c) Draw the boundary between the linear and velocity saturation regions on the output $I$-$V$ characteristics of the NMOS transistor. Clearly label the relevant points. How does it compare to the model?

d) We will try to extract the parameters $V_{Th}$ and $\alpha$ for the alpha-power-law model $I_D = K(V_{GS} - V_{Th})^\alpha$ from SPICE simulations. Use Matlab to determine $K$, $V_{Th}$ and $\alpha$ (hint: use the $\text{lsqcurvefit}$ function). Determine the parameters for both NMOS and PMOS transistors.

e) By setting $\alpha = 1$, find the best $V_{Th}$'s that correspond to linear dependence of current on $V_{GS}$.

Solution (contributed by Pi-Feng Chiu)

a) Circuit Setup for $I_D$-$V_{GS}$ curve:
$|V_{DS}| = 50 \text{ mV}$, sweep $V_{GS}$ from 0 to 1.05V. Pick a point in linear section and draw the tangent line in MATLAB to calculate the intersection with x-axis.

In the model card,
$vth0\_n105 = vth0\_n105\_g + p\_vta$
$vth0\_n105\_g = '0.44216 + dvth0\_n105\_fc + dvth0\_n105\_mc + dvth0\_n105\_skew'$
$(p\_vta, dvth0\_n105\_fc, dvth0\_n105\_mc, dvth0\_n105\_skew=0)$
So $vth0\_n105 = 0.44216 \text{ V}$ (non-voltage-dependent threshold voltage).
b) Find the values of $E_{CL}$ that fit the NMOS/PMOS characterization

$$I_{DSat} = \frac{W}{L} \frac{\mu_{eff} C_{ox} E_{C} L}{2} \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_{CL}} (1 + \lambda V_{DS})$$

The equation is valid under saturation ($V_{DS} > V_{DSat}$). So I set $V_{DS}$=1.05V in this problem. I made some assumptions to fit the curve.

1) Finite output resistance: Calculate $\lambda$ at $V_{DS} = V_{GS} = 1.05V$ ($\lambda = \frac{g_{ds}}{I_D}$)

2) Calculate $\mu_{eff} C_{ox}$ from $gm$ derived in .OP results at $V_{DS} = V_{GS} = 1.05V$ , and assume $V_{GS} - V_{TH} >> E_{CL}$. (You can also just set $u_{Cox}$ as another fit parameter)

$$gm = \frac{dI_{DSat}}{dV_{GS}} = \frac{W}{L} \frac{\mu_{eff} C_{ox} E_{C} L}{2}$$

3) Change $E_{CL}$ and $V_{TH}$ to fit the curve:
In high $V_{DS}$, $V_{TH}$ would be reduce by DIBL
$\Rightarrow V_{TH}' = V_{TH} - \zeta V_{DS}$

NMOS

PMOS
c) Draw boundary of linear and velocity saturation regions.

\[ V_{DSAT} = \frac{(V_{GS} - V_{TH})E_{CL}L}{(V_{GS} - V_{TH}) + E_{CL}L} \]

I use \( V_{DSAT} \) to calculate \( V_{DSAT} \), with \( E_{CL}=0.8 \), \( V_{TH}=0.12 \) V in prob. 1b. The results are labeled on the plot. Compare to the model: extracting \( V_{DSAT} \) value in the .OP result, \( V_{DSAT} = 239, 284, 330, 377, 424 \), respectively. The difference could be due to the extracted \( V_{TH} \) is lower than in the model card.

d) Curve-fitting for alpha-power-law model:

\[ I_D = K(V_{GS} - V_{Th})^\alpha \]
2. Transistor sizing

a) Using SPICE and 32nm LP model with 1.05V supply, find the required width of the PMOS transistor that minimizes the propagation delay \( (t_{pHL} + t_{pLH})/2 \) for the CMOS inverter. NMOS transistor width is 100nm.
b) Optimally size the CMOS NAND2 gate. Find the required width (W) for the NMOS transistors in the pull-down such that the equivalent resistance of the pull-down network is the same as the equivalent resistance of the pull down transistor in an inverter from part a). Use hand analysis with parameters from Problem 1. (In case you haven’t been able to solve Problem 1, you can use $E_{CL} = 0.8V$, $V_{DD} = 1V$, and $V_{Th} = 0.5V$). Compare with SPICE and discuss any discrepancies.

c) Repeat part b) for a NAND3 gate. Compare with SPICE and discuss any discrepancies.

d) Optimally size NOR2 gate by using SPICE to match the inverter form part a).

Solution (contributed by Pi-Feng Chiu)

1. Transistor sizing
   a) Find the required width of PMOS for minimum propagation delay
      @ NMOS size: 100nm/32nm
      Using SPICE to sweep over PMOS width with FO4:

      ![Graph showing the relationship between PMOS width and delay]

      \(\Rightarrow\) The minimum propagation delay happens at PMOS width = 170nm

   b) Optimally size the CMOS NAND2 gate. Find the required width (W) for NMOS transistors in the pull-down.
      Hand Calculation:
      \[
      I_{DSat} = \frac{W \mu_{eff} C_{ox} E_{CL}}{2} \left( \frac{V_{GS} - V_{Th}}{V_{GS} - V_{Th}} + E_{CL} \right)
      \]
      In inverter case –
      \[
      I_{DSat, inv} = \frac{W \mu_{eff} C_{ox} E_{CL}}{2} \left( \frac{V_{GS} - V_{Th}}{V_{GS} - V_{Th}} + E_{CL} \right)
      \]
      In NAND2 case –
      \[
      I_{DSat, NAND2} = \frac{W \mu_{eff} C_{ox}}{2L} \frac{2(E_{CL})}{2} \left( \frac{V_{GS} - V_{Th}}{V_{GS} - V_{Th}} + 2(E_{CL}) \right)
      \]
      Set $ECL = 0.8$, $V_{Th} = 0.12$ (from problem 1(b))
\[
\frac{I_{DSat,inv}}{I_{DSat,NAND2}} = \frac{(V_{GS} - V_{Th}) + 2E_cL}{(V_{GS} - V_{Th}) + E_cL} = 1.46
\]

NMOS width = 146nm to meet the requirement. (Solve for W required to increase NAND2 current to the same level)

Simulation:
NMOS width = 204nm to meet the requirement. (Another way to solve for optimum width would be to plot the total propagation delay vs. width, but this would be less likely to agree with the hand calculation.)

The simulation result shows the NMOS width needs to be larger than the value from hand calculation. The discrepancy is largely due to different $E_cL$ and $V_{TH}$ extraction.

c) Optimally size the CMOS NAND3 gate

Hand Calculation:
\[
\frac{I_{DSat,inv}}{I_{DSat,NAND2}} = \frac{(V_{GS} - V_{Th}) + 3E_cL}{(V_{GS} - V_{Th}) + E_cL} = 1.92
\]

NMOS width = 192nm to meet the requirement.

Simulation:
NMOS width = 335nm to meet the requirement.

The simulation result shows the NMOS width needs to be larger than the value from hand calculation. The discrepancy is largely due to different $E_cL$ and $V_{TH}$ extraction.

d) Optimally size NOR2:
Size the stacked PMOS to have the same resistance as in the inverter.

Hand Calculation:
Set $E_cL = 1.48$, $V_{Th} = 0.15$ (for PMOS from problem 1(b))
\[
\frac{I_{DSat.inv}}{I_{DSat.NOR2}} = \frac{(V_{GS} - V_{Th}) + 2E_c L}{(V_{GS} - V_{Th}) + E_c L} = 1.62
\]

PMOS width: 1.62*170nm = 275 nm (NMOS width remains 100nm)

Simulation:
NMOS width = 310nm to meet the requirement.

The simulation result shows a smaller difference than in NMOS cases. It might be because of better coefficient extraction.

3. Design a 4-to-16 decoder using a typical VLSI flow

a) Work through GCD: VLSI's Hello World (on the course website), a brief tutorial that will describe how industry tools translate RTL code to final layout. Try to understand the high-level concepts of what is happening and don't worry too much about the details for now. Turn in:

- The first 45 lines of the post-place-and-route Verilog netlist

b) In your /scratch/username directory on icluster[9-12].eecs.berkeley, type:

```
source ~/ee241/tutorials/ee241.bashrc
git clone ~/ee241/tutorials/decoder
```

Edit src/decoder.v, and write a verilog description of a 4-to-16 decoder. Open src/decoder_testbench.v (a test bench we wrote for you) and try to understand the file. Next, edit build/constraints.tcl and build/Makefrag and describe the following constraints: 30fF load capacitance on each output pin, inputs driven by a minimum sized inverter, and target maximum frequency. Then synthesis, place-and-route, and test the design (de-
syn/, icc-par/, vcs-sim-gl-par/), and turn in:

- A screenshot of the layout
- The critical path in ns
- A post P&R DVE simulation waveform showing correct functionality and the critical path

Solution (contributed by Stevo Bailey)
Problem 3

a)

Post PAR verilog netlist result:

```
module gcdGCDUnitCtrl (clk , reset , operands_val , result_rdy , B_zero ,
    A_lt_B , result_val , operands_rdy , A_mux_sel , B_mux_sel , A_en ,
    B_en , IN0 , IN1 );
input clk ;
input reset ;
input operands_val ;
input result_rdy ;
input B_zero ;
input A_lt_B ;
output result_val ;
output operands_rdy ;
output [1:0] A_mux_sel ;
output B_mux_sel ;
output A_en ;
output B_en ;
input IN0 ;
input IN1 ;
wire [1:0] state ;
```
Figure 14: Decoder Layout

<table>
<thead>
<tr>
<th>Point</th>
<th>Fanout</th>
<th>Cap</th>
<th>Trans</th>
<th>Incr</th>
<th>Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>clock ideal_clock1 (rise edge)</td>
<td></td>
<td></td>
<td>0.0000</td>
<td>0.0000</td>
<td></td>
</tr>
<tr>
<td>clock network delay (ideal)</td>
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<td>0.0000</td>
<td>0.0000</td>
<td></td>
</tr>
<tr>
<td>input external delay</td>
<td></td>
<td></td>
<td>0.0000</td>
<td>0.0000 r</td>
<td></td>
</tr>
<tr>
<td>A[3] (in)</td>
<td>0.0196</td>
<td>0.0098</td>
<td>0.0098 r</td>
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<td></td>
</tr>
<tr>
<td>A[3] (net)</td>
<td>4</td>
<td>3.5621</td>
<td>0.0000</td>
<td>0.0000 r</td>
<td></td>
</tr>
<tr>
<td>U39/A (INVX1_RVT)</td>
<td>0.0196</td>
<td>0.0000 &amp;</td>
<td>0.0099 r</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U39/Y (INVX1_RVT)</td>
<td>0.0142</td>
<td>0.0113</td>
<td>0.0212 f</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n31 (net)</td>
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<td>0.7404</td>
<td>0.0000</td>
<td>0.0212 f</td>
<td></td>
</tr>
<tr>
<td>U37/A1 (AND2X1_RVT)</td>
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<td>0.0000 &amp;</td>
<td>0.0212 f</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U37/Y (AND2X1_RVT)</td>
<td>0.0309</td>
<td>0.0413</td>
<td>0.0625 f</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n18 (net)</td>
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<td>4.0203</td>
<td>0.0000</td>
<td>0.0625 f</td>
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</tr>
<tr>
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<td>0.0001 &amp;</td>
<td>0.0626 f</td>
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<td></td>
</tr>
<tr>
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<td>0.1060 f</td>
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<td>0.0368</td>
<td>0.1428 f</td>
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</tr>
<tr>
<td>icc_route_opt30/Y (NBUFFX16_RVT)</td>
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<td>0.0368</td>
<td>0.1428 f</td>
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<td></td>
</tr>
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<td>Z[5] (net)</td>
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<td>0.0000</td>
<td>0.1430 f</td>
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</tr>
<tr>
<td>Z[5] (out)</td>
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<td>0.0001 &amp;</td>
<td>0.1430 f</td>
<td></td>
<td></td>
</tr>
<tr>
<td>data arrival time</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>clock ideal_clock1 (rise edge)</td>
<td>0.0500</td>
<td>0.0500</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>clock network delay (ideal)</td>
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<td>0.0500</td>
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<tr>
<td>clock reconvergence pessimism</td>
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<td>0.0500</td>
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<td></td>
</tr>
<tr>
<td>data required time</td>
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<td></td>
</tr>
<tr>
<td>data required time</td>
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<td></td>
</tr>
<tr>
<td>data arrival time</td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

slack (VIOLATED) -0.0930
Figure 15: Decoder testbench waveform showing correct functionality
Figure 16: Decoder critical path waveform showing transition from A[3] to Z[5]