1. Extracting and simulating the synthesized design.

In the first lab, we have created a design by using a strictly digital (‘VLSI’) design flow. Then in the second lab, we extracted and simulated the synthesized design using custom design tools. In this third lab we will close the loop and build the remaining part of the flow where we will characterize a custom cell for use in the synthesis flow.

To do this, please work through the tutorial entitled: *Introduction to the Custom Design Flow: Building a standard cell*, then turn in:

a) Report the critical path of the 4-to-16 decoder reported by IC Compiler before and after using your new NAND2 cell. Attach a layout of your cell placed inside IC Compiler (set level=99 to see inside the instance).

b) Using a Monte Carlo simulation of 300 points, plot the mean and sigma for the input-rising/output-fall delay of INVX0\_RVT (10ps input slope, 1fF load) for VDD between 0.2 and 1 on the same plot. Then plot \( \sigma/\mu \) vs. VDD on another plot. Lastly, plot the delay of a 6\( \sigma \) cell relative to the mean vs. VDD on a third plot. Explain conceptually why variation has more of an effect at low voltages.

c) Generate a histogram of the delay at 0.6V and at 1.05V and try to fit a normal curve (use histfit in Matlab). Are either of them Gaussian? If a distribution is asymmetric, explain why one side has the long tail and not the other. (Optional: use the qqplot command to compare two vectors: one vector from your simulations, and the other sampled from a normal distribution with the \( \mu \) and \( \sigma \) found from the fit using normrnd)

d) Compute \( \sigma_{\text{Vth}} \) for the NMOS in INVX0\_RVT. Then, using Ion from the alpha-power-law model (\( K=1.7e-4, \ V_{\text{th}}=0.366, \alpha=1.36 \)), write out the equation for the delay of an inverter (simply assuming maximum current for a transition from VDD to VDD/2 is close enough: \( \Delta T = C \Delta V/I \), where \( \Delta V = \text{VDD/2} \) and \( C \) is approximately 1.5fF). Then use Matlab to run a Monte Carlo simulation on this model for 0.6V and 1.05V by using normrnd with a \( \mu=0 \) and \( \sigma=\sigma_{\text{Vth}} \) and adding this value to the threshold (which is exactly what HSPICE is doing for Monte Carlo simulation, but HSPICE is solving more complex equations). How do the distributions compare to part c)? Based on the equation you wrote, should the delay be Gaussian?

2. Timing

For this question, use the circuit shown in Figure 1. The numbers in the blocks represent combinational logic delays (in ps) between the latches and flip-flops. The clock-to-q delay of the latches and flip-flops are included in the combinational delays, and both latches and flip-flops have a setup time of 100ps. Assume that the clock has a 50% duty cycle.
a) What is the minimum clock period at which the circuit in Figure 1 will operate correctly? Assume that there is no skew. Please show all work (particularly timing diagrams, if you rely on them).

b) What is the new minimum period if only L1 has a clock skew of 75ps? What is the new minimum period if only L2 has a clock skew of 75ps? Justify your answers.

3. Flip-flops
Two flip-flop designs are shown in Fig. 2. A design from Fig. 2b. attempts to improve over the traditional design from Fig. 2a. Compare the clock-to-output delay, setup times, hold times and the switching energy of the two designs. Assume that both are optimally sized for fastest operation.