Problem 1:

Problem 2:

Problem 3:

Problem 4:

Total:
PROBLEM 1. (10 pts) Sizing.

a) (5 pts) For the NAND2 gate in Figure 1.b, determine the width of the top NMOS, \( w \), such that the \( t_{\text{pHL}} \) is equivalent to that of the inverter in Figure 1.a. All transistors are minimum length, and the widths are in \( \mu \text{m} \).

\[
V_{\text{DD}} = 1\text{V}, V_{\text{Th}} = 0.3\text{V}, E_CL = 0.7\text{V} \text{ (for NMOS)}, I_{\text{DSat}} = 1\text{mA/\mu m} \text{ (} V_{\text{GS}}=V_{\text{DD}}\text{)}, L=50\text{nm}.
\]

\[
I_{\text{DSat}} = \frac{W \mu_{\text{eff}} C_{\text{ox}} E_C L}{2} \left( \frac{(V_{GS} - V_{Th})^2}{(V_{GS} - V_{Th}) + E_CL} \right)
\]

\[
V_{\text{DSat}} = \frac{(V_{GS} - V_{Th}) E_CL}{(V_{GS} - V_{Th}) + E_CL}
\]
b) (5pts) For the NAND2 gate in Figure 1.c, determine the width of the bottom NMOS, w, such that the $t_{phL}$ is equivalent to that of the inverter in Figure 1.a. All transistors are minimum length, and the widths are in $\mu$m.
PROBLEM 2. (10 pts) SRAM
A 10-T SRAM cell is shown in Figure 2. It has one read and one write port, and uses a single-ended read and a differential write. There are two wordlines, one used for read and one for write operation.

<table>
<thead>
<tr>
<th>RWL</th>
<th>WWL</th>
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<tbody>
<tr>
<td>WWL</td>
<td>VDD</td>
</tr>
</tbody>
</table>

a) (5 pts) How should the transistors in this cell be sized to guarantee read stability and writeability, with minimum area at nominal supply voltages? Please explain.
b) (5 pts) What is the key advantage of this cell, compared to the standard 8T SRAM cell with one read and one write port, in terms of area, speed, dynamic or static power?
PROBLEM 3. (10 pts) Dynamic logic.

Figure 3 shows an illustration of so called “limited-switch dynamic logic” style. Logic function is implemented in the ‘nfet logic’ block.

![Diagram of a 2-input XOR gate in limited-switch dynamic logic style.](image)

a) (6 pts) Show an implementation of a 2-input XOR gate in this logic style. Only true logic inputs are available (no complements).
b) (4 pts) List three main differences between this logic style and the conventional domino logic. Explain your answer.
PROBLEM 4. (12 pts) Adders.

In this problem, we will examine some properties of carry-lookahead adders.

Figure 4.

a) (4 pts) What is the radix of the Ladner-Fischer carry-lookahead tree from Figure 4? Explain your answer.
b) (4 pts) Draw a domino implementation of logic inside the box marked in Figure 4 (in the second and third stage above inputs $A_7$ and $B_7$). Assume conventional carry-lookahead implementation in footless domino logic. Please label all inputs and outputs.
c) (4 pts) Draw a sparse version of the Ladner-Fischer tree from Figure 4. Every second carry should be calculated. Highlight the critical path in this figure.