Problem 1:

Problem 2:

Problem 3:

Problem 4:

Total:
PROBLEM 1. (12 pts) Sizing.

For this problem, all transistors are minimum length. Technology parameters are given below:

\[ V_{DD} = 1V, \ V_{Th} = 0.4V, \ L=25\text{nm}. \] Effective mobility is two times higher in NMOS devices.

<table>
<thead>
<tr>
<th>NMOS</th>
<th>PMOS</th>
</tr>
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<tbody>
<tr>
<td>(E_{CL} = 0.6V, \ I_{DSat} = 1mA/\mu m \ (V_{GS}=V_{DD}=1V))</td>
<td>(E_{CL} \to \infty, \ I_{DSat} = 1mA/\mu m \ (V_{GS}=V_{DD}=1V))</td>
</tr>
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\[
I_{DSat} = \frac{W \ \mu_{eff} C_{ox} E_{CL} L}{2} \left( \frac{(V_{GS}-V_{Th})^2}{(V_{GS}-V_{Th})+E_{CL}} \right)
\]

\[
V_{DSat} = \frac{(V_{GS}-V_{Th}) E_{CL}}{(V_{GS}-V_{Th})+E_{CL}}
\]

a) (4pts) What is the optimal sizing of PMOS transistor in an inverter with NMOS width of \(W_n = 100\text{nm}\)?
b) (4pts) What should be the optimal sizing of transistors in a 3-input NAND gate, compared to a unit-sized inverter from part a)? Doing an approximate calculation is fine.

c) (4pts) What should be the optimal sizing of transistors in a 2-input NOR gate, compared to a unit-sized inverter from part a)? Doing an approximate calculation is fine.
PROBLEM 2. (10 pts) SRAM
Consider a conventional 6-T SRAM cell is shown in Figure 2.a. It is sized to be stable under nominal conditions.

![Figure 2.a.](image)

a) (6 pts) How does the higher WL voltage affect the:
   - Read stability
   - Read access time
   - Half-select condition

Explain your answer.
b) (4pts) Some designers use a “delayed WL boost” technique, illustrated in Figure 2.b. Explain the reasoning for using such a waveform.

Figure 2.b.
PROBLEM 3. (10 pts) Dynamic logic.

Figure 3 shows an illustration of so called “limited-switch dynamic logic” style. Logic function is implemented in the ‘nfet logic’ block.

![Limited-switch dynamic logic](image)

Figure 3.

a) (6 pts) Show an implementation of a 2-input XOR gate in this logic style. Only true logic inputs are available (no complements).
b) (4 pts) List three main differences between this logic style and the conventional domino logic. Explain your answer.
PROBLEM 4. (16 pts) Timing

For this question, use the circuit shown in Figure 1. The numbers in the blocks represent combinational logic delays (in ps) between the latches and flip-flops. The clock-to-q delay of the latches and flip-flops are included in the combinational delays, and both latches and flip-flops have a setup time of 100ps. Assume that the clock has a 50% duty cycle.

a) (8pts) What is the minimum clock period at which the circuit in Figure 1 will operate correctly? Assume that there is no skew. Please show all work (particularly timing diagrams, if you rely on them).
b) (8 pts) What is the new minimum period if only L1 has a clock skew of 75ps? What is the new minimum period if only L2 has a clock skew of 75ps? Justify your answers. Note: if you did not answer the first part, discuss when skew affects the minimum period in a latch-based system. Give examples to justify your claims.