Announcements

› Homework 2 due next week
Outline

› Last lecture
  › Dynamic margins
  › Started assist techniques

› This lecture
  › Assist techniques

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SRAM

E. Assist Techniques (continued)
Array Adjustments

Array back bias, to compensate for systematic variations

May be useful in technologies with strong body effect

S. Mukhopadhyay, VLSI 2006

Dynamic V_{DD} Implementation

VCC selection is along column direction to decouple the read & write

Zhang, ISSCC'05
Floating VDD Technique

- W/o second supply

Collapsing $V_{DD}$ Technique

Yamaoka, ISSCC’04

E. Karl, ISSCC’12
Collapsing $V_{DD}$ Technique

E. Karl, ISSCC’12

Negative BL Write Assist

Nii, VLSI’08
Negative BL

BL Stability Assist

Arsovski, ISSCC'11
WL Underdrive

- Sensing appropriate WL voltage

Carlson, CICC'08

Nho, ISSCC'10

Capacitive Write Assist

S. Ohbayashi, VLSI 2006
Write/Read Assist

H. Pilo, VLSI 2006

Pulsed WL/BL

M. Khellah, VLSI 2006
Pulsing WL

Wordline pulse shape

Generating boost

Sinangil, ISSCC’2011

SRAM Periphery Design

Did not discuss:
- Hierarchical bitlines
- Optimal sense-amp triggering
- Sense-amplifier design