Announcements

- Homework 2 due on Wednesday
- Quiz #2 on Wednesday
- Midterm project report due next Week (4 pages)

  - Title
  - Authors
  - Abstract (5 sentences)
  - Introduction
  - Problem statement
  - Solutions to the problem
  - Your proposed solution/comparison/metric
  - How will you prove it? Expected results
  - Conclusion
  - References

EE241 - Spring 2013
Advanced Digital Integrated Circuits

Lecture 12: SRAM Design – ECC Timing
Reading

› H. Partovi, “Clocked storage elements,” Ch. 11 in Design of High-Performance Microprocessor Circuits, by Chandrakasan, Bowhill, Fox

Outline

› Last lecture
  › SRAM assist techniques

› This lecture
  › ECC in SRAM
  › Back to timing
SRAM

F. Redundancy and ECC

Multi-bit Errors


Model used in circuit simulation

Model used in device simulation

Kawahara, ISSCC'07 tutorial
Multi-bit Errors

Kawahara, ISSCC'07 tutorial
Multi-bit Errors: Interleaving

Placement at alternate addresses

Ref.: K. Osada et al., [12].

SRAM

G. Options for scaling
SRAM Scaling

- Approaching fundamental limits:
  - Don’t scale cell size
  - Increase transistor count (from 6)
  - Change technology (e.g. double-gate FETs)
    - eDRAM
    - ReRAM
  - Or something else…

Vmin Scaling Projections

- Itoh, ISSCC’09
SRAM Alternatives

8-T SRAM

- Dual-port read/write capability (register file-like cells)
- N0, N1 separates read and write
  - No Read SNM constraint
  - Half-selected cells still undergo read stress – no single cell write capability
- Stacked transistors reduce leakage

L. Chang, VLSI Circuits 2005

Alternatives: Thin-Body MOSFETs

- Thin body suppresses short channel effects
  - Channel lightly doped → higher carrier mobility
  - $T_{OX}$ scaling not needed → less reliability issues
- Double-gate structure is scalable to $L_g < 10$nm
6-FinFET SRAM Cell

175mV nominal SNM w/ 0.36µm² cell area (45nm)

6-FinFET SRAM Cell: 2 Fins

240mV SNM w/ 0.42µm² cell area
36% SNM improvement w/ 17% area penalty
**Bulk-Si FinFETs**

Lee, *VLSI*’04, Kavaleros, *VLSI*’06

- FinFETs can be made on bulk-Si wafers
  - lower cost
  - improved thermal conduction to mitigate self-heating effects
  - integration with planar bulk-Si MOSFETs is possible

**eDRAM**

Process cost: Added trench capacitor

Barth, ISSCC’07, Wang, IEDM’06