Announcements

› Homework 3 due on Monday
› Quiz #3 on Monday
› Makeup lecture on Friday, 3pm, in 540AB
Outline

› Last lecture
  › Flip-flops

› This lecture
  › Finish flip-flops
  › Power issues

4. Design for performance

C. Latches and flip-flops (continued)
Pulse-Triggered Latches

7474, from mid-1960’s

First stage is a sense amplifier, precharged to high, when Clk = 0
After rising edge of the clock sense amplifier generates the pulse on S or R
The pulse is captured in S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges

DEC Alpha 21264, StrongARM 110
Sense Amplifier-Based Flip-Flop

Sampling Window Comparison

Naffziger, JSSC 11/02
Some Interesting Questions

- How to compare delays analytically?
  - Similar to LE
  - Analytical setup time
- How to evaluate robustness analytically?

4. Design for Performance
   D. Robustness in Timing
Shadow Latch Concept

If flip-flop fails to capture the data, there will be an error signal generated by the latch.

Razor I Issues

- Good idea but has a few issues:

  - Improved idea:
Other Realizations

▶ Razor II
   Das, JSSC'09

▶ Transition detector with time borrowing (TDTB)
   Bowman, JSSC'09

Several other ideas

5. Low Power Design
Performance Optimization

Increasing performance increases power!

Microarchitecture A

Microarchitecture B
How to Increase Performance?

- **Scale technology**
- **Circuit level:**
  - Transistor sizing, buffering
  - Wire optimization, repeaters
  - Supply voltage
  - Threshold voltage
  - Logic styles
  - Timing, latches
- **Microarchitecture**
  - Block topologies (adders, multipliers)
  - Pipelining
  - Parallelism

Sizing Logic Paths for Speed

- Remember the method of logical effort
- For minimum delay, all gates should have the same effort (fg)
- Optimal effort for a gate is around 4
5. Low Power Design
A. Power and Energy Basics

Importance of Power Awareness

- **Energy: Crucial for Portable Applications**
  - Determines battery lifetime
  - Amount of computation
  - Performance is what sells products

- **Power: Crucial for High-Performance Applications**
  - Determines cooling and energy costs
  - Many designs today are power limited
  - Still need maximum performance
Portability: Battery Limits

- Little change in basic technology
- Store energy using a chemical reaction
- Battery capacity doubles every 10 years
  - Has slowed down
- Energy density/size, safe handling are limiting factor

<table>
<thead>
<tr>
<th>Energy density of material</th>
<th>KWH/kg</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gasoline</td>
<td>14</td>
</tr>
<tr>
<td>Lead-Acid</td>
<td>0.04</td>
</tr>
<tr>
<td>Li polymer</td>
<td>0.15</td>
</tr>
</tbody>
</table>

Battery Progress

- Energy Density (Wh/kg)
- Trend Line

First Commercial Use

- NiCd
- SLA
- NiMH
- Li-Ion
- Reusable Alkaline
- Li-Polymer
Know Your Enemy

- Where does power go in CMOS?
- **Switching (dynamic) power**
  - Charging capacitors
- **Leakage power**
  - Transistors are imperfect switches
- **Short-circuit power**
  - Both pull-up and pull-down on during transition
- **Static currents**
  - Biasing currents

5. Low Power Design
B. Power-Performance Tradeoffs
Achieve the highest performance under the power cap

Design optimization curves

Achieve the highest performance under the power cap
Achieve the highest performance under the power cap

How far away are we from the optimal solution?
**Power-Performance Optimization**

Global optimum – best performance

Maximize throughput for given energy or
Minimize energy for given throughput
There are many sets of parameters to adjust

Tuning variables

- Circuit  
  (sizing, supply, threshold)
- Logic style  
  (std. cells, custom , ...)
- Block topology  
  (adder: CLA, CSA, ...)
- Micro-architecture  
  (parallel, pipelined)

Globally optimal power-performance curve for a given function
Next Lecture

- Power-performance tradeoffs at circuit level