EE241 - Spring 2013
Advanced Digital Integrated Circuits

Lecture 18: Dynamic Voltage Scaling

Announcements

- Homework 3 due today
- Quiz #3 today
Reading


Outline

› Last lecture
  › Power-performance tradeoffs at circuit level
  › Tradeoffs through supply voltage

› This lecture
  › Multiple supplies
  › Dynamic voltage scaling
5. Low Power Design
F. Multiple Supplies

<table>
<thead>
<tr>
<th></th>
<th>Constant Throughput/Latency</th>
<th>Variable Throughput/Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Energy</strong></td>
<td>Design Time</td>
<td>Sleep Mode</td>
</tr>
<tr>
<td><strong>Active</strong></td>
<td>Logic design</td>
<td>Clock gating</td>
</tr>
<tr>
<td></td>
<td>Scaled $V_{DD}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Trans. sizing</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Multi-$V_{DD}$</td>
<td></td>
</tr>
<tr>
<td><strong>Leakage</strong></td>
<td>Stack effects</td>
<td>Sleep T's</td>
</tr>
<tr>
<td></td>
<td>Trans sizing</td>
<td>Multi-$V_{DD}$ Variable $V_{Th}$</td>
</tr>
<tr>
<td></td>
<td>Scaling $V_{DD}$</td>
<td>+ Input control</td>
</tr>
<tr>
<td></td>
<td>+ Multi-$V_{Th}$</td>
<td></td>
</tr>
</tbody>
</table>
Reducing Active Power

- Downsizing, lowering the supply on the critical path will lower the operating frequency
- Downsize (lowering supply) non-critical paths
  - Narrows down the path delay distribution
  - Increases impact of variations

Multiple Supply Voltages

- Block-level supply assignment
  - Higher throughput/lower latency functions are implemented in higher $V_{DD}$
  - Slower functions are implemented with lower $V_{DD}$
  - Often called “Voltage islands”
  - Separate supply grids, level conversion performed at block boundaries
- Multiple supplies inside a block
  - Non-critical paths moved to lower supply voltage
  - Level conversion within the block
  - Physical design challenging
Leakage Issue

Driving from $V_{DDL}$ to $V_{DDH}$  
Level converter

Multiple Supplies in a Block

Conventional Design  
CVS Structure

Lower $V_{DD}$ portion is shaded  
“Clustered voltage scaling”  

M. Takahashi, ISSCC’98.
Multiple Supplies in a Block

CVS

Layout:

Level-Converting Flip-Flop

Usami'98
From Two to Three $V_{DD}$'s

From Kuroda

$V_1 = 1.5V$, $V_{TH} = 0.3V$, $\rho(t)$: lambda

Optimum Numbers of Supplies

The more $V_{DD}$'s, the less power, but the effect will be saturated.

Power reduction effect will be decreased as $V_{DD}$'s are scaled.

Optimum $V_2/V_1$ is around 0.7.

Hamada, CICC'01
## 5. Low Power Design
### G. Dynamic Voltage Scaling

### Power /Energy Optimization Space

<table>
<thead>
<tr>
<th></th>
<th>Constant Throughput/Latency</th>
<th>Variable Throughput/Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Energy</strong></td>
<td>Design Time</td>
<td>Sleep Mode</td>
</tr>
<tr>
<td><strong>Active</strong></td>
<td>Logic design</td>
<td>Clock gating</td>
</tr>
<tr>
<td></td>
<td>Scaled $V_{DD}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Trans. sizing</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Multi-$V_{DD}$</td>
<td></td>
</tr>
<tr>
<td><strong>Leakage</strong></td>
<td>Stack effects</td>
<td>Sleep T's</td>
</tr>
<tr>
<td></td>
<td>Trans sizing</td>
<td>Multi-$V_{DD}$ Variable $V_{Th}$</td>
</tr>
<tr>
<td></td>
<td>Scaling $V_{DD}$</td>
<td>+ Input control</td>
</tr>
<tr>
<td></td>
<td>+ Multi-$V_{Th}$</td>
<td></td>
</tr>
</tbody>
</table>
Adaptive Supply Voltages

Exploit Data Dependent Computation Times To Vary the Supply

from [Nielsen94]

(IEEE Transactions on VLSI Systems)

Processors for Portable Devices

- Eliminate performance ↔ energy trade-off
Typical MPEG IDCT Histogram

Number of IDCTs per Frame

Frequency of Occurrence

0.00 0.02 0.04 0.06

0 500 1000 1500 2000

Processor Usage Model

Desired Throughput

Compute-intensive and low-latency processes

Maximum Processor Speed

SystemIdle

Background and high-latency processes

System Optimizations:
• Maximize Peak Throughput
• Minimize Average Energy/operation
**Common Design Approaches (Fixed VDD)**

- **Compute ASAP:**
  - Delivered Throughput
  - Always high throughput
  - Excess throughput

- **Clock Frequency Reduction:**
  - $f_{CLK}$ Reduced
  - Energy/operation remains unchanged while throughput scaled down with $f_{CLK}$

**Scale $V_{DD}$ with Clock Frequency**

- Constant supply voltage
- $\sim 10x$ Energy Reduction
- Reduce $V_{DD}$, slow circuits down.

**Chart:**
- Throughput ($\propto f_{CLK}$)
- Energy/operation
- $1.1V$ vs $3.3V$
CMOS Circuits Track Over $V_{DD}$

Delay tracks within +/- 10%

Dynamic Voltage Scaling (DVS)

1. Vary $f_{CLK}$, $V_{DD}$
2. Dynamically adapt

- Dynamically scale energy/operation with throughput.
- Always minimize speed $\rightarrow$ minimize average energy/operation.
- Extend battery life up to 10x with the exact same hardware!
Operating System Sets Processor Speed

- DVS requires a voltage scheduler (VS).
- VS predicts workload to estimate CPU cycles.
- Applications supply completion deadlines.

\[ \frac{\text{CPU cycles}}{\Delta \text{time}} = F_{\text{DESIREDE}} \]

Converter Loop Sets V\text{DD}, f\text{CLK}

- Feedback loop sets V\text{DD} so that \( F_{\text{ERR}} \rightarrow 0 \).
- Ring oscillator delay-matched to CPU critical paths.
- Custom loop implementation → Can optimize \( C_{\text{DD}} \).
Next Lecture

› Continue DVS