Announcements

- Homework 1 due today
- Homework 2 posted this week
Reading

- J. Chang, et al, “A 20nm 112Mb SRAM Design in High K/Metal Gate Technology with Assist Circuitry for Low Leakage and Low Vmin Applications,” ISSCC’13
- K. Zhang et al (Springer)
- K. Loh et al (Elsevier)

Outline

- Last lecture
  - Static timing
  - Variability in design
- This lecture
  - Variability
  - SRAM operation
I. Design Variability

Some systematic effects

Layout: Poly Proximity Effects

- Gate CD is a function of its neighborhood
  - Light intensity profile falling on the resist
  - Resist: application of developer fluid\(^1\), post exposure bake (PEB) temperature\(^2\)
  - Dry etching: microscopic loading effects\(^3\)

- Gate length depends on

\[^1\] J. Cain, M.S. Thesis, UC Berkeley
Layout: Proximity Test Structures

90nm experiments
- Single gate inverter layout
- Dummy poly
- Stacked gates

45nm experiments
- No single gates allowed

L.T. Pang, VLST'06
L.T. Pang, CICC'08

Ring oscillators and individual transistor leakage currents

Results: Single Gates in 90nm

- Max $\Delta F$ between layouts $> 10$
- Within-die $3\sigma/\mu$ $\sim$ 3.5%, weak dependency on density

L.T. Pang, VLST'06
L.T. Pang, CICC'08

36 chips, 4632 data points

Fastest
Slowest
Results: Single Gates in 45nm

- Weak effect on performance. $\Delta F \sim 2\%$
- Small shifts in NMOS leakage and bigger shifts in PMOS leakage

Impact of Stress

- 45nm STM process: Wafer rotated $<100>$ - higher PMOS mobility
- NMOS strained through capping layer
- Subatmospheric STI – weak tensile stress
Impact of Longer Diffusion in 45nm

- Strongest effect measured in 45nm, $\Delta F \sim 5\%$
- No significant shift in $I_{\text{LEAK}}$

Impact of Shallow Trench Isolation (STI)

- $\Delta F \sim 3\%$, small changes in $I_{\text{LEAK}}$
- Due to STI-induced stress
Chip Yield Depends on Inter-Gate Correlation

Yield = \text{Pr}(\text{sum of } n \text{ delays} < \text{clock period})

\begin{align*}
\rho = 0 \text{ gives highest yield through averaging} \\
\text{Non-correlated gates in a path reduce impact of variation}
\end{align*}

Bowman et al, JSSC, Feb 2002.
Chip Yield Depends on Inter-Path Correlation

Yield = Pr (max delay of K paths < clock period)
K = 1 gives highest yield

Correlated paths reduce impact of variation

Bowman et al, JSSC, Feb 2002

J. Design Variability

Some random effects
Random Dopant Fluctuations

Number of dopants is finite

Frank, IBM J R&D 2002
Processing: Line-Edge Roughness

- Sources of line-edge roughness:
  - Fluctuations in the total dose due to quantization
  - Resist composition
  - Absorption positions

Effect:
- Variation (random) in leakage and power

Oxide Thickness

- Systematic variations +
- Roughness in the Si./SiO2 interface
- Smaller effect than RDF

Asenov, TED’2002
Transistor Matching

Transistor $V_{TH}$s vary with size ($\sim \sqrt{WL}$) and distance

![Graph showing the relationship between $V_{TH}$ and $1/\sqrt{(WL)}$ for different technologies.]

Pelgrom parameter $A_{VT}$
- Scales with technology (EOT)

\[ A_{VT} \sim 2.1 \quad \text{(bulk Si)} \]

$A_{VT}$ in FDSOI technology
\[ \sim 28 \quad \text{(32 nm)} \]


Negative Bias Temperature Instability

PFET $V_{TH}$'s shift in time, at high negative bias and elevated temperatures

The mechanism is thought to be the breaking of hydrogen-silicon bonds at the Si/SiO2 interface, creating surface traps and injecting positive hydrogen-related species into the oxide.

Also other charge trapping and hot-carrier defect generation

Systematic + random shifts

Tsujikawa, IRPS'2003
Random Telegraph Signal (RTS)

- Trapping of a carrier in oxide traps modulates $V_{th}$ or $I_{ds}$
- $\tau_e$ and $\tau_c$ are random and follow exponential distributions


RTS and Technology Scaling

$\Delta V_{th, RTS} \sim \frac{1}{WL}$

$\Delta V_{th, RDF} \sim \frac{1}{\sqrt{WL}}$

$\Delta V_{th}$ (mV)

CDF ($\sigma$)

L/W = 20/45nm

$\Delta V_{th}$ (mV)

Tega et. al, VLSI Tech. 09

» RTS exceeds RDF at 3 sigma in the 22nm node