EE241 - Spring 2013
Advanced Digital Integrated Circuits

Lecture 9: SRAM Design

Announcements

› Homework 2 posted this week
› Quiz #1 on Monday
Outline

- Last lecture
  - Finished variability
- This lecture
  - SRAM operation

Part 3: SRAM

A. Basics
SRAM Topics

A. Basics and trends
B. Static margins
C. Dynamic margins
D. Assist techniques
E. Periphery, redundancy and error correction
F. Scaling options

SRAM Scaling Trends

- Individual SRAM cell area able to track ITRS guideline
- Array area deviates from ITRS guideline at 90nm
- Memory design no longer sits on the 0.5x area scaling trend!
**6-T SRAM Cell**

- Improve CD control by unidirectional poly
- Relax critical layer patterning requirements
- Optimizing design rules is key

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**SRAM Cell Design Trends**

- Key enabling technology:
- Impact:

  - Cell in 90nm (1μm²)
  - Cell in 32nm (0.171μm²)
More SRAM Trends

- 0.15μm² cell in 32nm from TSMC (IEDM'07)
- 0.1μm² cell in 22nm from IBM (IEDM'08)

SRAM Cell Trends (22nm)

A little analysis using a ruler:
- Aspect ratio 2.9
- Height ~178nm, Width ~518nm
- Gate ~ 45nm (Lg is smaller)

- 0.092μm² cell in 22nm from Intel (IDF'09)
- 0.346μm² cell in 45nm from Intel (IEDM'07)
22nm SRAM

- FinFET cell design

SRAM

B. Static Retention Margin
SRAM Cell/Array

- Hold (retention) stability
- Read stability
- Write stability
- Read current (access time)

Access Transistor

Pull down
Pull up

SRAM Design – Hold (Retention) Stability

- Scaling trend:
  - Increased gate leakage + degraded $I_{ON}/I_{OFF}$ ratio
  - Lower $V_{DD}$ during standby
  - PMOS load devices must compensate for leakage
Retrieval Stability

- Would like to reduce supply in standby

Monte-Carlo Simulation of DRV Distribution

Simulated DRV of 1500 SRAM cells (mV)

Qin, ISQED'04
Vmin Distribution

- Alternative to static margin characterization
- Digital test under supply sweep

SRAM

C. Static Read/Write Margins
6T-SRAM Array Basics – Read Operation

Read Stability – Static Noise Margin (SNM)

- Read SNM is the contention between the two sides of the cell under read stress.

$$\Delta V_{th} \propto \frac{1}{C_{ox} \sqrt{WL}}$$

Due to RDF
Read SNM - Measurements

Read margin vs. retention margin
Bhavnagarwala, IEDM’05

Read Stability – N-Curve

- A, B, and C correspond to the two stable points A and C and the meta-stable point B of the SNM curve
- When points A and B coincide, the cell is at the edge of stability and a destructive read can occur

Grossar, JSSC’06
Write Stability – Write Noise Margin (WNM)

- Writeability is becoming harder with scaling
- Optimizing read stability and writeability at the same time is difficult

A. Bhavnagarwala, IEDM 2005
Write Stability – BL/WL Write Margins

- Highest BL voltage under which write is possible when BLC is kept precharged
- Difference between VDD and lowest WL voltage under which write is possible when both bit-lines are precharged

Write Stability – Write Current (N-Curve)

- Minimum current into the storage node
The Conflict Between Read and Write

6-T SRAM Static/Dynamic Stability

- **Read Margin**
  - SNM: pessimistic
- **Write Margin**
  - WNM: optimistic
- Introduction to dynamic margins
**SRAM**

Dynamic Write Stability

- $T_A < T_{\text{write}} < T_B$
- $T_{\text{write}}$ = dynamic write stability
- Static margins are optimistic

Khalil, TVLSI’08
**Dynamic Read Stability**

- $T_A < T_{\text{read}} < T_B$
- $T_{\text{read}} =$ dynamic read stability
- Static margins are pessimistic

Khalil, TVLSI ’08

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**Dynamic Read Access**

- $T_A < T_{\text{access}} < T_B$
- PD₁ and PG₁ are critical

Khalil, TVLSI ’08
**V_{Th} Window**

- Assuming global spread

![Graph showing V_{Th} Window with pMOS and nMOS threshold voltages](attachment:graph.png)

Yamaoka, ISSCC’05

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**Next Lecture**

- Continue with SRAM