Administrative

- Elad will be out of town this Thurs.
  - Make-up lecture will be held on Mon. 1-31 1:30-3:00pm in 127 Dwinelle
  - Office hours on Thurs. cancelled – available over email
Plain Old Inverters – Why Not?

Outline

- Signaling Basics
  - Single-ended vs. differential
  - “Current-mode” vs. “Voltage-mode” signaling
  - Termination

- TX Circuit Design
  - Z control
  - CML, VM drivers
  - Power vs. swing
  - Serialization options

- RX Circuit Design
  - Comparator review
  - Deserialization options
### Single-Ended Signaling

- **RX**: comparing against a shared reference
  - Reference may be implicit (i.e., ground/supply)
  - Mismatch between shared and individual lines
- **TX**: generates large variations on power supply
  - SSO – simultaneous switching outputs
- **No XTALK immunity**

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**So Why Even Mention This?**
Classic Debate

- “Differential must be twice as fast as single-ended in order to win”

- Reality more complicated
  - E.g., power supply to signaling pin ratio higher in S.E.

- Short “answer”
  - Differential a lot easier to build and get right the first time
  - Can make S.E. work – but often a lot more painful

“Voltage-Mode” vs. ”Current-Mode”

- Transmission line has both voltage and current...
- Terminology unfortunately heavily overloaded
  - Whether or not Zo of driver is high
  - How Zo of driver is set
  - What sets output swing
"Voltage-Mode" vs. "Current-Mode"

Another View

<table>
<thead>
<tr>
<th></th>
<th>&quot;Low Impedance&quot;</th>
<th>&quot;High Impedance&quot;</th>
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</thead>
<tbody>
<tr>
<td><strong>Single Ended</strong></td>
<td><img src="image1" alt="Diagram" /></td>
<td><img src="image2" alt="Diagram" /></td>
</tr>
<tr>
<td><strong>V_s</strong></td>
<td><img src="image3" alt="Diagram" /></td>
<td><img src="image4" alt="Diagram" /></td>
</tr>
<tr>
<td><strong>V_s/2</strong></td>
<td><img src="image5" alt="Diagram" /></td>
<td><img src="image6" alt="Diagram" /></td>
</tr>
<tr>
<td><strong>Shared</strong></td>
<td><img src="image7" alt="Diagram" /></td>
<td><img src="image8" alt="Diagram" /></td>
</tr>
<tr>
<td><strong>Differential</strong></td>
<td><img src="image9" alt="Diagram" /></td>
<td><img src="image10" alt="Diagram" /></td>
</tr>
</tbody>
</table>

- RX opposite of TX
- Signal integrity implications?
Why Terminate?

External vs. Internal Termination

- **Internal**: makes package L, pad C part of T-line
- **External**: chip/package become a stub
  - If want on-die term need to control its value…
Untrimmed Poly Termination

- Main issue is variation: +/-20% at one temperature
- But
  - It’s relatively linear
  - ESD robust
  - Low parasitics...

Ri, Ci, and Pad Complexity

- LPF at pad can dominate overall channel
- Example: 500fF ESD, 500fF driver, 500fF wire
  - Bandwidth ~4GHz with double-terminated link
- Even worse in busses (or if add big series R)...
Active Terminations

AC vs. DC Termination

- With diff. can terminate to complement
  - High Z $\rightarrow$ lower power
  - See more shortly

- TX sets common-mode
  - Can be inconvenient
  - May need wide CM range

- AC-coupled + AC-term
  - Places some requirements on data though
TX Design: Series vs. Parallel Termination

Alphabet Soup

• LVDS, CML
• GTL, GTL+, RSL, ...

• VM, CM
• HCM, LCM

• All same basic principles
  • Look at two representative circuits to understand some of the more fundamental tradeoffs
CML TX + RX Term

Double-terminated on-chip

Side Note: Pre-Driver
CML Power Consumption

Differential VM TX + RX

- Main motivation: can reduce power for same swing/supply
Simplified Model And Power

Bad News: Extra Complexity

- Driver impedance (termination) now set totally by devices
  - Some sort of impedance control is critical

- “High-swing” driver:
Low-Swing VM Driver

- Old standards often required large swings (>1V diff. p2p)
  - More modern designs use much lower swings (~200-400mV diff. p2p) to save power

- Low-swing VM driver:

Impedance Control
Another Approach

Serialization: Input vs. Output

- On-chip clocks often slower than off-chip data-rates
  - Need to take a set of parallel on-chip data and serialize it

- Can serialize either at input of TX or at final output
Serialization: Input vs. Output

• Input ser. requires on-chip circuitry to run at full line rate
  • May lead to high power consumption
  • In older technologies (0.35um) was hard to support high-freq. clocks

• Output ser. noved burden at pad
  • At the time was highest BW

• Limit in both designs: edge rate
  • Either for the clock or for the data

Basic TX Final Notes

• Usually need many peripheral controls
  • Zo, edge-rate, etc.

• Keep tuning out of the high-speed signal path
  • P(High-speed, low res. + low-speed, high-res.) << P(high-speed, high-res.)
Basic TX Final Notes

• Lots of research focused on reduced signaling power
  • I.e., power spent by actual final driver

• Watch out for “overhead” (pre-drivers)
  • Especially with emerging low-swing designs, overhead can actually dominate
    • $P_{\text{sig}}$ (400mV diff. p2p):
    • $P_{\text{digital}}$ (100 min. sized inverters @ 10GHz):

• More on this later

Basic RX

• Simplest: RX is just a comparator @ $f_{\text{bit}}$
  • (Clocking later)

• Key things to watch out for:
  • High sensitivity (low noise, low offset/hysteresis)
  • Common-mode input range
  • Supply/common-mode rejection
  • Max. clock rate
  • Power consumption
Typical Design

StrongArm Review
Higher Speeds