CTLE Review

- Generally implemented on RX
  - (Higher Z than TX – less power for same V swing/gain)
CTLE Review: Circuit Design

• Most common design: source-degenerated

Source-Degenerated CTLE In Practice

• Several issues to watch out for
  • Finite input device $r_o$
  • Tail node $r_o$, $C_{par}$
  • Self loading/BW limits
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FIR Equalizer

• Most often implemented at the TX
  • Delay is easy – just need flip-flops

• Typical mixed-signal implementation:
TX FIR Direct Implementation

- FIR coefficients generally not fixed
  - Depend on channel, temp., process, etc.
- Direct approach very flexible
  - But can have high parasitics (self-loading) – especially with large number of taps

Fundamental Problem
Alternate Approach with Min. $C_{par}$

A Middle Ground

- Partition segments based on knowledge of possible coefficients*

- Tradeoff between
  - $C_{par} \rightarrow$ analog BW, power
  - Digital complexity, power

- “Optimum” point depends on technology, data-rate
  - Generally don’t want to focus on just the end points

What About VM Drivers?