CTLE Review

- Generally implemented on RX
  - (Higher Z than TX – less power for same V swing/gain)

CTLE Review: Circuit Design

- Most common design: source-degenerated

Source-Degenerated CTLE In Practice

- Several issues to watch out for
  - Finite input device $r_s$
  - Tail node $r_o$, $C_{par}$
  - Self loading/BW limits

FIR Equalizer

- Most often implemented at the TX
  - Delay is easy – just need flip-flops

- Typical mixed-signal implementation:

\[
\begin{align*}
data_in & \rightarrow & \text{sgn1} \rightarrow & V_{out} \\
\end{align*}
\]
TX FIR Direct Implementation

- FIR coefficients generally not fixed
  - Depend on channel, temp., process, etc.
- Direct approach very flexible
  - But can have high parasitics (self-loading) – especially with large number of taps

A Middle Ground

- Partition segments based on knowledge of possible coefficients
- Tradeoff between
  - $C_{par}$ → analog BW, power
  - Digital complexity, power
- “Optimum” point depends on technology, data-rate
  - Generally don’t want to focus on just the end points

Fundamental Problem

Alternate Approach with Min. $C_{par}$

What About VM Drivers?