A Few Real Stories…

- Missing bias current
- Inverted feedback
A Few Real Stories…

- Bus order swapped
- Even/odd flip

A Few Real Stories…

- 2's vs. 1’s complement
How to Catch In Simulation?

• Check DC operating point?

• Transient with full transistor netlist?

How to Catch In Simulation?

• Mixed-mode simulation with transistor netlist for analog blocks?

• Mixed-mode simulation with verilogA models?
Analog Modeling with HDLs

• Key advantage: HDL simulators are event-driven
  • Compute only when something happens

• Other advantages:
  • Easy to port
  • Single environment for control (digital) & datapath (analog) verification

Ref: C. Werner, CICC 2005

Pin-Compatibility

• HDL and schematic views must be pin-compatible
  • Too many chances for errors to slip through otherwise
  • Allows full vs. behavioral sim from single database

• Choose schematic boundaries/hierarchy wisely…
Behavioral Analog in HDL Basics

- Model analog quantities with (32-bit) integers
  - Pick voltage/current resolution a priori
  - (E.g., 1µV/1nA)

- Often requires netlist post-processing
  - Convert single-wire analog quantities into 32-bit bus
  - May also need type conversions (I to V, V to I) in schematic

Simple Example

```vhdl
/* %%% SCHEMATIC START %%% */
module rfc_mbsseg (out, outb, d, db, itail);
  output out, outb;
  input d, db;
  input itail;
endmodule
/* %%% SCHEMATIC END %%% */

/* %%% GLM START %%% */
module rfc_mbsseg (out, outb, d, db, itail);
  output[31:0] out, outb;
  input d, db;
  input[31:0] itail;
  integer ibias, diff, out, outb;
  always @(d or db or itail) begin
    ibias = itail*4;
    out = (d => db) ? 0 : -ibias;
    outb = (d > db) ? -ibias : 0;
  end
endmodule
/* %%% GLM END %%% */
```

from C. Werner, CICC 2005
Example #2

```
always @(d or PowerDown or IMasterBias) begin
  if (PowerDown == 1) begin
    iout = 0;
    end
  else begin
    iout = (1-d[0])*1 + (1-d[1])*2 + (1-d[2])*4 + (1-d[3])*8;
    iout = (iout * IMasterBias)/16;
  end
end
```

from C. Werner, CICC 2005

Current Summation
Current Summation cont’d

Example #3

```
begin
  event=clk_in;
  case (en[5:0])
    7'b0000000: #(0*BitTime/256);
    7'b0000001: #(1*BitTime/256);
    7'b0000010: #(2*BitTime/256);
    ...
    7'b111111: #(63*BitTime/256);
  endcase
  clk_out=event;
end
```

from C. Werner, CICC 2005
Channel Modeling

Some Take-Home Lessons
A Final Warning