A Few Real Stories...
- Missing bias current
- Inverted feedback

How to Catch In Simulation?
- Check DC operating point?
- Transient with full transistor netlist?

A Few Real Stories...
- Bus order swapped
- Even/odd flip

How to Catch In Simulation?
- Mixed-mode simulation with transistor netlist for analog blocks?
- Mixed-mode simulation with verilogA models?
Analog Modeling with HDLs

- Key advantage: HDL simulators are event-driven
  - Compute only when something happens

- Other advantages:
  - Easy to port
  - Single environment for control (digital) & datapath (analog) verification

Ref: C. Werner, CICC 2005

Pin-Compatibility

- HDL and schematic views must be pin-compatible
  - Too many chances for errors to slip through otherwise
  - Allows full vs. behavioral sim from single database

- Choose schematic boundaries/hierarchy wisely...

Behavioral Analog in HDL Basics

- Model analog quantities with (32-bit) integers
  - Pick voltage/current resolution a priori
    - (E.g., 1µV/1nA)

- Often requires netlist post-processing
  - Convert single-wire analog quantities into 32-bit bus
  - May also need type conversions (I to V, V to I) in schematic

Simple Example

```vhdl
// #\$ SCHEMATIC START #\$ /
module ref_mosaic (out, outb, d, db, itall);
  output out, outb;
  input d, db;
  input [1:0] itall;
  endmodule
// #\$ SCHEMATIC END #\$ /

// #\$ GX MSTART #\$ /
module ref_mosaic (out, outb, d, db, itall);
  output [1:0] out, outb;
  input d, db;
  input [1:0] itall;
  integer ibias, diff, out, outb;
  always @ (d or db or itall begin
    ibias = itall*4;
    out = (d + db) ? 0 : -ibias;
    outb = (d + db) ? -ibias : 0;
  end
  endmodule
// #\$ GX END #\$ /
```

Example #2

```vhdl
always @ (d or PowerDown or IMasterBias) begin
  if (PowerDown == 1) begin
    iout = 0;
  end
  else begin
    iout = (1 - d[0]) * 1 + (1 - d[1]) * 2 +
          (1 - d[2]) * 4 + (1 - d[3]) * 8;
    iout = iout * IMasterBias / 16;
  end
end
```

Current Summation
Current Summation cont'd

Example #3

```
begin
  eventclk k;
  case (e[k]):
  7'b0000000: #0*BitTime/256;
  7'b0000001: #1*BitTime/256;
  7'b0000010: #2*BitTime/256;
  ...
  7'b1111111: #63*BitTime/256);
  endcase
  3k_out_event;
end
```
from C. Werner, CICC 2005

A Final Warning

Some Take-Home Lessons

Channel Modeling